# Multi-Threshold CMOS Digital Circuits

Managing Leakage Power

Mohab Anis Mohamed Elmasry

# <u>Multithreshold Cmos Digital Circuits Managing Leakage</u> <u>Power</u>

**Patrick Lee** 

# **Multithreshold Cmos Digital Circuits Managing Leakage Power:**

Multi-Threshold CMOS Digital Circuits Mohab Anis, Mohamed I. Elmasry, 2003-10-31 This excellent survey of state of the art techniques discusses the MTCMOS technology that has emerged as an increasingly popular technique to control the escalating leakage power while maintaining high performance It addresses the leakage problem in a number of designs for combinational sequential dynamic and current steering logic Multi-Threshold Cmos Digital Circuits: Managing Leakage Power Anis, 2009-10-01 Multi-Threshold CMOS Digital Circuits Mohab Anis, Mohamed Elmasry, 2012-12-06 Multi Threshold CMOS Digital Circuits Managing Leakage Power discusses the Multi threshold voltage CMOS MTCMOS technology that has emerged as an increasingly popular technique to control the escalating leakage power while maintaining high performance The book addresses the leakage problem in a number of designs for combinational sequential dynamic and current steering logic Moreover computer aided design methodologies for designing low leakage integrated circuits are presented The book give an excellent survey of state of the art techniques presented in the literature as well as proposed designs that minimize leakage power while achieving high performance Multi Threshold CMOS Digital Circuits Managing Leakage Power is written for students of VLSI design as well as practicing circuit designers system designers CAD tool developers and researchers It assumes a basic knowledge of digital circuit design and device operation and covers a broad range of circuit design techniques Communication and Networking Tai-hoon Kim, Hojjat Adeli, Wai-chi Fang, Thanos Vasilakos, Adrian Stoica, Charalampos Z. Patrikakis, Gansen Zhao, Javier Garcia Villalba, Yang Xiao, 2011-12-03 The two volume set CCIS 265 and 266 constitutes the refereed proceedings of the International Conference FGCN 2011 held as Part of the Future Generation Information Technology Conference FGIT 2011 Jeju Island Korea in December 2011 The papers presented were carefully reviewed and selected from numerous submissions and focuse on the various aspects of future generation communication and networking Introduction to Low-Power Design in VLSIs Patrick Lee, 2011-12-12 This book discusses one increasingly important issue in the VLSI design low power It covers the following topics a basic concepts of low power design b low power design methods and applications in industry chips and c commercial CAD tools on low power design This book discusses the concepts a set of known methods industry cases and CAD tools on the low power design It is organized in four chapters and a glossary is provided at the end of the book *Integrated Circuit and System Design Enrico* Macii, Vassilis Paliouras, Odysseas Koufopavlou, 2004-09-07 This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation PATMOS 2004 held in Santorini Greece in September 2004 The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted The papers are organized in topical sections on buses and communication circuits and devices low power issues architectures asynchronous circuits systems design interconnect and physical design security and safety low power processing digital design and modeling and simulation **Extreme Low-Power Mixed Signal IC** 

**Design** Armin Tajalli, Yusuf Leblebici, 2010-09-14 Design exibility and power consumption in addition to the cost have always been the most important issues in design of integrated circuits ICs and are the main concerns of this research as well Energy Consumptions Power dissipation P and energy consumption are diss pecially important when there is a limited amount of power budgetor limited source of energy Very common examples are portable systems where the battery life time depends on system power consumption Many different techniques have been veloped to reduce or manage the circuit power consumption in this type of systems Ultra low power ULP applications are another examples where power dissipation is the primary design issue In such applications the power budget is so restricted that very special circuit and system level design techniquesare needed to satisfy the requirements Circuits employed in applications such as wireless sensor networks WSN wearable battery powered systems 1 and implantable circuits for biol ical applications need to consume very low amount of power such that the entire system can survive for a very long time without the need for changingor recharging battery 2.4 Using newpowersupplytechniques such as energy harvesting 5 and printable batteries 6 is another reason for reducing power dissipation Devel ing special design techniques for implementing low power circuits 7 9 as well as dynamic power management DPM schemes 10 are the two main approaches to control the system power consumption Design Flexibility Design exibility is the other important issue in modern in grated systems Advanced Computing Natarajan Meghanathan, B.K. Kaushik, Dhinaharan Nagamalai, 2010-12-14 This volume constitutes the third of three parts of the refereed proceedings of the First International Conference on Computer Science and Information Technology CCSIT 2010 held in Bangalore India in January 2011 The 46 revised full papers presented in this volume were carefully reviewed and selected The papers are organized in topical sections on soft computing such as AI Neural Networks Fuzzy Systems etc distributed and parallel systems and algorithms security and information assurance ad hoc and ubiquitous computing wireless ad hoc networks and sensor networks Power Management of Digital Circuits in Deep Sub-Micron CMOS <u>Technologies</u> Stephan Henzler, 2006-11-24 In the deep sub micron regime the power consumption has become one of the most important issues for competitive design of digital circuits Due to dramatically increasing leakage currents the power consumption does not take advantage of technology scaling as before State of art power reduction techniques like the use of multiple supply and threshold voltages transistor stack forcing and power gating are discussed with respect to implementation and power saving capability Focus is given especially on technology dependencies process variations and technology scaling Design and implementation issues are discussed with respect to the trade off between power reduction performance degradation and system level constraints A complete top down design flow is demonstrated for power gating techniques introducing new design methodologies for the switch sizing task and circuit blocks for data retention and block activation The leakage reduction ratio and the minimum power down time are introduced as figures of merit to describe the power gating technique on system level and give a relation to physical circuit parameters Power Management of Digital

Circuits in Deep Sub Micron CMOS Technologies mainly deals with circuit design but also addresses the interface between circuit and system level design on the one side and between circuit and physical design on the other side **Soft Error Mechanisms, Modeling and Mitigation** Selahattin Sayil,2016-02-25 This book introduces readers to various radiation soft error mechanisms such as soft delays radiation induced clock jitter and pulses and single event SE coupling induced effects In addition to discussing various radiation hardening techniques for combinational logic the author also describes new mitigation strategies targeting commercial designs Coverage includes novel soft error mitigation techniques such as the Dynamic Threshold Technique and Soft Error Filtering based on Transmission gate with varied gate and body bias The discussion also includes modeling of SE crosstalk noise delay and speed up effects Various mitigation strategies to eliminate SE coupling effects are also introduced Coverage also includes the reliability of low power energy efficient designs and the impact of leakage power consumption optimizations on soft error robustness The author presents an analysis of various power optimization techniques enabling readers to make design choices that reduce static power consumption and improve soft error reliability at the same time

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