

Multilevel Interconnection Technology Without Via-Hole Mask (Maskless Pillar Process)

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SUMMARY

Recently, with the miniaturization of ULSI patterns, the percentage of the LSI production cost occupied by the multilevel interconnection process is increasing due to the increase in the process steps and the introduction of new materials. In order to realize miniaturization process and achieve cost reduction at the same time, via-hole maskless multilevel interconnect technology (maskless pillar process) has been developed. By merging the via-hole mask information on the underlying interconnection mask and by a selective etching of the multilevel metal films which depends on the mask width, underlying interconnection and metal pillars are formed simultaneously. The reduction of process steps has become possible by eliminating the via-hole lithography, etching, and filling process. As a result of electrical measurement of samples formed by the maskless pillar process, the feasibility for two-level metal interconnection has been verified, which confirmed it to be a multilevel interconnection process suitable for sub-half micron devices with guaranteed reliability.

Key words: Multilevel interconnection; low cost; via-hole; pillar.

1. Introduction

Recently, with the miniaturization of ULSI patterns, the production cost shows an increasing trend due

to the increase of process steps and the introduction of new materials and new equipment. Furthermore, the multilevel interconnection has a problem of throughput reduction associated with the increase of the interconnection levels, the use of multilayers for interconnection structure, and the use of new technique for metal filling of small contacts and via holes.

Among new recent approaches on the miniaturized multilevel interconnection technology, DUAL DAMASCENE method [1] and using chemical-mechanical polishing (CMP) technique and a method to form via holes and interconnection at the same time using self-aligned plug [2] are proposed. Although these methods are superior in the self-alignment of via holes and interconnection, they require metal filling. On the other hand, there is a method [3, 4] to form a pillar (metal pillar) without filling technique. However, all the methods above require two photolithography steps to form a via hole and an interconnection and do not achieve process step reduction. Although an example to reduce the mask levels in multilevel interconnect process has been presented in the literature [5], it tends to increase the total number of steps.

The new multilevel interconnection technology in this work realizes a fine process and at the same time reduces the process steps dramatically by the combination of a conventional technique and a conventional equipment. The via-hole specific mask is eliminated by including the via-hole information into the underlying

Multilevel Interconnection Technology

Christoph Steinbruchel, Barry Chin



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Multilevel Interconnect Technology, 1998 **Multilevel Interconnect Technology** Gopal K. Rao, 1993 The first book on a key topic in IC technology Table of Contents Multilevel Interconnection Design Multilevel Interconnect Processing Manufacturing Reliability Index 100 illustrations Multilevel Interconnection Hoang H. Hoang, 1993 **Advanced Interconnects for ULSI Technology** Mikhail Baklanov, Paul S. Ho, Ehrenfried Zschech, 2012-02-17 Finding new materials for copper low k interconnects is critical to the continuing development of computer chips While copper low k interconnects have served well allowing for the creation of Ultra Large Scale Integration ULSI devices which combine over a billion transistors onto a single chip the increased resistance and RC delay at the smaller scale has become a significant factor affecting chip performance Advanced Interconnects for ULSI Technology is dedicated to the materials and methods which might be suitable replacements It covers a broad range of topics from physical principles to design fabrication characterization and application of new materials for nano interconnects and discusses Interconnect functions characterisations electrical properties and wiring requirements Low k materials fundamentals advances and mechanical properties Conductive layers and barriers Integration and reliability including mechanical reliability electromigration and electrical breakdown New approaches including 3D optical wireless interchip and carbon based interconnects Intended for postgraduate students and researchers in academia and industry this book provides a critical overview of the enabling technology at the heart of the future development of computer chips *Handbook of Semiconductor Manufacturing Technology* Yoshio Nishi, Robert Doering, 2017-12-19 Retaining the comprehensive and in depth approach that cemented the bestselling first edition's place as a standard reference in the field the Handbook of Semiconductor Manufacturing Technology Second Edition features new and updated material that keeps it at the vanguard of today's most dynamic and rapidly growing field Iconic experts Robert Doering and Yoshio Nishi have again assembled a team of the world's leading specialists in every area of semiconductor manufacturing to provide the most reliable authoritative and industry leading information available Stay Current with the Latest Technologies In addition to updates to nearly every existing chapter this edition features five entirely new contributions on Silicon on insulator SOI materials and devices Supercritical CO₂ in semiconductor cleaning Low dielectrics Atomic layer deposition Damascene copper electroplating Effects of terrestrial radiation on integrated circuits ICs Reflecting rapid progress in many areas several chapters were heavily revised and updated and in some cases rewritten to reflect rapid advances in such areas as interconnect technologies gate dielectrics photomask fabrication IC packaging and 300 mm wafer fabrication While no book can be up to the minute with the advances in the semiconductor field the Handbook of Semiconductor Manufacturing Technology keeps the most important data methods tools and techniques close at hand A Multilevel Planar Interconnect Technology Utilizing the Selective Deposition of Tungsten David Charles Thomas, 1990 *Copper Interconnect Technology* Christoph Steinbrüchel, Barry

Chin, 2001 A textbook designed to accompany The Society of Photo Optical Instrumentation Engineers short course on improving interconnect performance for increased speed in overall circuit performance authored by Steinbrunel materials science and engineering Rensselaer Polytechnic Institute and Chin senior *Low Temperature Multilevel Interconnection Technology Employing a Polyimide* James William Peterson, 1985 **Copper Interconnect Technology** Tapan

Gupta, 2010-01-22 Since overall circuit performance has depended primarily on transistor properties previous efforts to enhance circuit and system speed were focused on transistors as well During the last decade however the parasitic resistance capacitance and inductance associated with interconnections began to influence circuit performance and will be the primary factors in the evolution of nanoscale ULSI technology Because metallic conductivity and resistance to electromigration of bulk copper Cu are better than aluminum use of copper and low k materials is now prevalent in the international microelectronics industry As the feature size of the Cu lines forming interconnects is scaled resistivity of the lines increases At the same time electromigration and stress induced voids due to increased current density become significant reliability issues Although copper low k technology has become fairly mature there is no single book available on the promise and challenges of these next generation technologies In this book a leader in the field describes advanced laser systems with lower radiation wavelengths photolithography materials and mathematical modeling approaches to address the challenges of Cu interconnect technology *Fundamentals of Semiconductor Processing Technology* Badih El-Kareh, Lou N. Hutter, 2012-12-06 The drive toward new semiconductor technologies is intricately related to market demands for cheaper smaller faster and more reliable circuits with lower power consumption The development of new processing tools and technologies is aimed at optimizing one or more of these requirements This goal can however only be achieved by a concerted effort between scientists engineers technicians and operators in research development and manufacturing It is therefore important that experts in specific disciplines such as device and circuit design understand the principle capabilities and limitations of tools and processing technologies It is also important that those working on specific unit processes such as lithography or hot processes be familiar with other unit processes used to manufacture the product Several excellent books have been published on the subject of process technologies These texts however cover subjects in too much detail or do not cover topics important to modern technologies This book is written with the need for a bridge between different disciplines in mind It is intended to present to engineers and scientists those parts of modern processing technologies that are of greatest importance to the design and manufacture of semiconductor circuits The material is presented with sufficient detail to understand and analyze interactions between processing and other semiconductor disciplines such as design of devices and circuits their electrical parameters reliability and yield

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