
On Optimal Interconnections for VLSI

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On Optimal Interconnections For Vlsi:

On Optimal Interconnections for VLSI Andrew B. Kahng, Gabriel Robins, 2013-04-17 On Optimal Interconnections for VLSI describes from a geometric perspective algorithms for high performance high density interconnections during the global and detailed routing phases of circuit layout First the book addresses area minimization with a focus on near optimal approximation algorithms for minimum cost Steiner routing In addition to practical implementations of recent methods the implications of recent results on spanning tree degree bounds and the method of Zelikovsky are discussed Second the book addresses delay minimization starting with a discussion of accurate yet algorithmically tractable delay models Recent minimum delay constructions are highlighted including provably good cost radius tradeoffs critical sink routing algorithms Elmore delay optimal routing graph Steiner arborescences non tree routing and wiresizing Third the book addresses skew minimization for clock routing and prescribed delay routing formulations The discussion starts with early matching based constructions and goes on to treat zero skew routing with provably minimum wirelength as well as planar clock routing Finally the book concludes with a discussion of multiple competing objectives i e how to optimize area delay skew and other objectives simultaneously These techniques are useful when the routing instance has heterogeneous resources or is highly congested as in FPGA routing multi chip packaging and very dense layouts Throughout the book the emphasis is on practical algorithms and a complete self contained development On Optimal Interconnections for VLSI will be of use to both circuit designers CAD tool users as well as researchers and developers in the area of performance driven physical design

Optimal Interconnection Trees in the Plane Marcus Brazil, Martin Zachariasen, 2015-04-13 This book explores fundamental aspects of geometric network optimisation with applications to a variety of real world problems It presents for the first time in the literature a cohesive mathematical framework within which the properties of such optimal interconnection networks can be understood across a wide range of metrics and cost functions The book makes use of this mathematical theory to develop efficient algorithms for constructing such networks with an emphasis on exact solutions Marcus Brazil and Martin Zachariasen focus principally on the geometric structure of optimal interconnection networks also known as Steiner trees in the plane They show readers how an understanding of this structure can lead to practical exact algorithms for constructing such trees The book also details numerous breakthroughs in this area over the past 20 years features clearly written proofs and is supported by 135 colour and 15 black and white figures It will help graduate students working mathematicians engineers and computer scientists to understand the principles required for designing interconnection networks in the plane that are as cost efficient as possible On-Chip Communication Architectures Sudeep Pasricha, Nikil Dutt, 2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have

been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that will have a significant impact on research and design of communication architectures over the next several years Handbook of Algorithms for Physical Design Automation Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, 2008-11-12 The physical design flow of any project depends upon the size of the design the technology the number of designers the clock frequency and the time to do the design As technology advances and design styles change physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in technology Handbook of Algorithms for Physical Design Automation provides a detailed overview of VLSI physical design automation emphasizing state of the art techniques trends and improvements that have emerged during the previous decade After a brief introduction to the modern physical design problem basic algorithmic techniques and partitioning the book discusses significant advances in floorplanning representations and describes recent formulations of the floorplanning problem The text also addresses issues of placement net layout and optimization routing multiple signal nets manufacturability physical synthesis special nets and designing for specialized technologies It includes a personal perspective from Ralph Otten as he looks back on the major technical milestones in the history of physical design automation Although several books on this topic are currently available most are either too broad or out of date Alternatively proceedings and journal articles are valuable resources for researchers in this area but the material is widely dispersed in the literature This handbook pulls together a broad variety of perspectives on the most challenging problems in the field and focuses on emerging problems and research results *Timing Analysis and Optimization of Sequential Circuits* Naresh Maheshwari, S. Sapatnekar, 2012-12-06 Recent years have seen rapid strides in the level of sophistication of VLSI circuits On the performance front there is a vital need for techniques to design fast low power chips with minimum area for increasingly complex systems while on the economic side there is the vastly increased pressure of time to market These pressures have made the use of CAD tools mandatory in designing complex systems Timing Analysis and Optimization of Sequential Circuits describes CAD algorithms for analyzing and optimizing the timing behavior

of sequential circuits with special reference to performance parameters such as power and area A unified approach to performance analysis and optimization of sequential circuits is presented The state of the art in timing analysis and optimization techniques is described for circuits using edge triggered or level sensitive memory elements Specific emphasis is placed on two methods that are true sequential timing optimizations techniques retiming and clock skew optimization Timing Analysis and Optimization of Sequential Circuits covers the following topics Algorithms for sequential timing analysis Fast algorithms for clock skew optimization and their applications Efficient techniques for retiming large sequential circuits Coupling sequential and combinational optimizations Timing Analysis and Optimization of Sequential Circuits is written for graduate students researchers and professionals in the area of CAD for VLSI and VLSI circuit design **Formal Semantics**

for VHDL Carlos Delgado Kloos,P. Breuer,2012-12-06 It is recognized that formal design and verification methods are an important requirement for the attainment of high quality system designs The field has evolved enormously during the last few years resulting in the fact that formal design and verification methods are nowadays supported by several tools both commercial and academic If different tools and users are to generate and read the same language then it is necessary that the same semantics is assigned by them to all constructs and elements of the language The current IEEE standard VHDL language reference manual LRM tries to define VHDL as well as possible in a descriptive way explaining the semantics in English But rigor and clarity are very hard to maintain in a semantics defined in this way and that has already given rise to many misconceptions and contradictory interpretations Formal Semantics for VHDL is the first book that puts forward a cohesive set of semantics for the VHDL language The chapters describe several semantics each based on a different underlying formalism two of them use Petri nets as target language and two of them higher order logic Two use functional concepts and finally another uses the concept of evolving algebras Formal Semantics for VHDL is essential reading for researchers in formal methods and can be used as a text for an advanced course on the subject Network Optimization

Panos M. Pardalos,Donald W. Hearn,William W. Hager,2012-12-06 Network optimization is important in the modeling of problems and processes from such fields as engineering computer science operations research transportation telecommunication decision support systems manufacturing and airline scheduling Recent advances in data structures computer technology and algorithm development have made it possible to solve classes of network optimization problems that until recently were intractable The refereed papers in this volume reflect the interdisciplinary efforts of a large group of scientists from academia and industry to model and solve complicated large scale network optimization problems

Crosstalk in Modern On-Chip Interconnects B.K. Kaushik,V. Ramesh Kumar,Amalendu Patnaik,2016-04-06 The book provides accurate FDTD models for on chip interconnects covering most recent advancements in materials and design Furthermore depending on the geometry and physical configurations different electrical equivalent models for CNT and GNR based interconnects are presented Based on the electrical equivalent models the performance comparison among the Cu

CNT and GNR based interconnects are also discussed in the book The proposed models are validated with the HSPICE simulations The book introduces the current research scenario in the modeling of on chip interconnects It presents the structure properties and characteristics of graphene based on chip interconnects and the FDTD modeling of Cu based on chip interconnects The model considers the non linear effects of CMOS driver as well as the transmission line effects of interconnect line that includes coupling capacitance and mutual inductance effects In a more realistic manner the proposed model includes the effect of width dependent MFP of the MLGNR while taking into account the edge roughness

Three-Dimensional Integrated Circuit Design Vasilis F. Pavlidis, Ioannis Savidis, Eby G. Friedman, 2017-07-04 Three Dimensional Integrated Circuit Design Second Edition expands the original with more than twice as much new content adding the latest developments in circuit models temperature considerations power management memory issues and heterogeneous integration 3 D IC experts Pavlidis Savidis and Friedman cover the full product development cycle throughout the book emphasizing not only physical design but also algorithms and system level considerations to increase speed while conserving energy A handy comprehensive reference or a practical design guide this book provides effective solutions to specific challenging problems concerning the design of three dimensional integrated circuits Expanded with new chapters and updates throughout based on the latest research in 3 D integration Manufacturing techniques for 3 D ICs with TSVs Electrical modeling and closed form expressions of through silicon vias Substrate noise coupling in heterogeneous 3 D ICs Design of 3 D ICs with inductive links Synchronization in 3 D ICs Variation effects on 3 D ICs Correlation of WID variations for intra tier buffers and wires Offers practical guidance on designing 3 D heterogeneous systems Provides power delivery of 3 D ICs Demonstrates the use of 3 D ICs within heterogeneous systems that include a variety of materials devices processors GPU CPU integration and more Provides experimental case studies in power delivery synchronization and thermal characterization

Nano Interconnects Afreen Khursheed, Kavita Khare, 2021-12-23 This textbook comprehensively covers on chip interconnect dimension and application of carbon nanomaterials for modeling VLSI interconnect and buffer circuits It provides analysis of ultra low power high speed nano interconnects based on different facets such as material modeling circuit modeling and the adoption of repeater insertion strategies and measurement techniques It covers important topics including on chip interconnects interconnect modeling electrical impedance modeling of on chip interconnects modeling of repeater buffer and variability analysis Pedagogical features including solved problems and unsolved exercises are interspersed throughout the text for better understanding Aimed at senior undergraduate and graduate students in the field of electrical engineering electronics and communications engineering for courses on Advanced VLSI Interconnects Advanced VLSI Design VLSI Interconnects VLSI Design Automation and Techniques this book Provides comprehensive coverage of fundamental concepts related to nanotube transistors and interconnects Discusses properties and performance of practical nanotube devices and related applications Covers physical and electrical phenomena of carbon nanotubes as well as

applications enabled by this nanotechnology Discusses the structure properties and characteristics of graphene based on chip interconnect Examines interconnect power and interconnect delay issues arising due to downscaling of device size

Analytical Methodology of Tree Microstrip Interconnects Modelling For Signal Distribution Blaise

Ravelo,2019-11-21 This book focuses on the modelling methodology of microstrip interconnects discussing various structures of single input multiple output SIMO tree interconnects for signal integrity SI engineering Further it describes lumped and distributed transmission line elements based on single input single output SIMO models of symmetric and asymmetric trees and investigates more complicated phenomenon such as interbranch coupling The modelling approaches are based on the analytical methods using the Z Y and T matrices The established method enables the S parameters and voltage transfer function of SIMO tree to be determined Providing illustrative results with frequency and time domain analyses for each tree interconnect structure the book is a valuable resource for researchers engineers and graduate students in fields of analogue RF microwave digital and mixed circuit design SI and manufacturing engineering *Steiner Trees in Industry* Xiuzhen

Cheng,Ding-Zhu Du,2013-12-01 This book is a collection of articles studying various Steiner tree problems with applications in industries such as the design of electronic circuits computer networking telecommunication and perfect phylogeny The Steiner tree problem was initiated in the Euclidean plane Given a set of points in the Euclidean plane the shortest network interconnecting the points in the set is called the Steiner minimum tree The Steiner minimum tree may contain some vertices which are not the given points Those vertices are called Steiner points while the given points are called terminals The shortest network for three terminals was first studied by Fermat 1601 1665 Fermat proposed the problem of finding a point to minimize the total distance from it to three terminals in the Euclidean plane The direct generalization is to find a point to minimize the total distance from it to n terminals which is still called the Fermat problem today The Steiner minimum tree problem is an indirect generalization Schreiber in 1986 found that this generalization i e the Steiner minimum tree was first proposed by Gauss **Computing and Combinatorics** Xiaodong Hu,Jie Wang,2008-06-19 The refereed proceedings of the 14th Annual International Computing and Combinatorics Conference COCOON 2008 held in Dalian China in June 2008 The 66 revised full papers presented were carefully reviewed and selected from 172 submissions The papers are organized in topical sections on algorithms and data structures algorithmic game theory and online algorithms automata languages logic and computability combinatorics related to algorithms and complexity complexity theory cryptography reliability and security and database theory computational biology and bioinformatics computational algebra geometry and number theory graph drawing and information visualization graph theory and algorithms communication networks and optimization wireless network network optimization and scheduling problem Algorithms and Computation Tetsuo

Asano,2006-11-30 This book constitutes the refereed proceedings of the 17th International Symposium on Algorithms and Computation ISAAC 2006 held in Kolkata India December 2006 The 73 revised full papers cover algorithms and data

structures online algorithms approximation algorithm computational geometry computational complexity optimization and biology combinatorial optimization and quantum computing as well as distributed computing and cryptography *Scientific Computing in Electrical Engineering* Wilhelmus H. Schilders, E. Jan W. ter Maten, Stephan H. M. J. Houben, 2004-08-11 This book presents the proceedings of the 4th International Workshop Scientific Computing in Electrical Engineering held in Eindhoven The Netherlands from June 23-28 2002 This workshop followed three earlier workshops held in 1997 at the Darmstadt University of Technology in 1998 at the Weierstrass Institute for Applied Analysis and Stochastics and in 2000 at the University of Rostock The main topics of SCEE 2002 were computational electrodynamics circuit simulation and coupled problems The objective of the workshop which was mainly directed at mathematicians and electrical engineers was to bring together scientists from universities and industry with the goal of intensive discussions about modelling and numerical simulation of electronic circuits and electromagnetic fields A special feature was the Industry Day where distinguished speakers discussed the needs of industry in the field of computational electromagnetics and circuit simulation The book contains papers of invited and contributed talks as well as from poster presentations **Analysis and Design of**

Networks-on-Chip Under High Process Variation Rabab Ezz-Eldin, Magdy Ali El-Moursy, Hesham F. A. Hamed, 2015-12-16 This book describes in detail the impact of process variations on Network on Chip NoC performance The authors evaluate various NoC topologies under high process variation and explain the design of efficient NoCs with advanced technologies The discussion includes variation in logic and interconnect in order to evaluate the delay and throughput variation with different NoC topologies The authors describe an asynchronous router as a robust design to mitigate the impact of process variation in NoCs and the performance of different routing algorithms is determined with and without process variation for various traffic patterns Additionally a novel Process variation Delay and Congestion aware Routing algorithm PDCR is described for asynchronous NoC design which outperforms different adaptive routing algorithms in the average delay and saturation throughput for various traffic patterns Concurrent Computations Stuart K. Tewksbury, Bradley Dickinson, Stuart C.

Schwartz, 2012-12-06 The 1987 Princeton Workshop on Algorithm Architecture and Technology Issues for Models of Concurrent Computation was organized as an interdisciplinary work shop emphasizing current research directions toward concurrent computing systems With participants from several different fields of specialization the workshop covered a wide variety of topics though by no means a complete cross section of issues in this rapidly moving field The papers included in this book were prepared for the workshop and taken together provide a view of the broad range of issues and alternative directions being explored To organize the various papers the book has been divided into five parts Part I considers new technology directions Part II emphasizes underlying theoretical issues Communication issues which are addressed in the majority of papers are specifically highlighted in Part III Part IV includes papers stressing the fault tolerance and reliability of systems Finally Part V includes systems oriented papers where the system ranges from VLSI circuits through powerful

parallel computers Much of the initial planning of the workshop was completed through an informal AT T Bell Laboratories group consisting of Mehdi Hatamian Vijay Kumar Adri aan Ligtenberg Sailesh Rao P Subrahmanyam and myself We are grateful to Stuart Schwartz both for the support of Princeton University and for his orga nizing local arrangements for the workshop and to the members of the organizing committee whose recommendations for participants and discussion topics were par ticularly helpful A Rosenberg and A T *Interconnect Noise Optimization in Nanometer Technologies* Mohamed Elgamel, Magdy A. Bayoumi, 2006-03-20 Interconnect has become the dominating factor in determining system performance in nanometer technologies Dedicated to this subject Interconnect Noise Optimization in Nanometer Technologies provides insight and intuition into layout analysis and optimization for interconnect in high speed high complexity integrated circuits The authors bring together a wealth of information presenting a range of CAD algorithms and techniques for synthesizing and optimizing interconnect Practical aspects of the algorithms and the models are explained with sufficient details The book investigates the most effective parameters in layout optimization Different post layout optimization techniques with complexity analysis and benchmarks tests are provided The impact crosstalk noise and coupling on the wire delay is analyzed Parameters that affect signal integrity are also considered Error Control for Network-on-Chip Links Bo Fu, Paul Ampadu, 2011-10-09 This book provides readers with a comprehensive review of the state of the art in error control for Network on Chip NOC links Coverage includes detailed description of key issues in NOC error control faced by circuit and system designers as well as practical error control techniques to minimize the impact of these errors on system performance

Intelligent Information Technologies: Concepts, Methodologies, Tools, and Applications Sugumaran, Vijayan, 2007-11-30 This set compiles more than 240 chapters from the world s leading experts to provide a foundational body of research to drive further evolution and innovation of these next generation technologies and their applications of which scientific technological and commercial communities have only begun to scratch the surface

Immerse yourself in the artistry of words with is expressive creation, Immerse Yourself in **On Optimal Interconnections For Vlsi** . This ebook, presented in a PDF format (*), is a masterpiece that goes beyond conventional storytelling. Indulge your senses in prose, poetry, and knowledge. Download now to let the beauty of literature and artistry envelop your mind in a unique and expressive way.

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