

Low-Power Design Methodology - Motivations

- Minimize power
 - Reduce power in various modes of device operation
 - Dynamic power, leakage power, or total power
- Minimize time
 - Reduce power quickly
 - Complete the design in as little time as possible
 - Prevent downstream issues caused by LPD techniques
 - Avoid complicating timing and functional verification
- Minimize effort
 - Reduce power efficiently
 - Complete the design with as few resources as possible
 - Prevent downstream issues caused by LPD techniques
 - Avoid complicating timing and functional verification

Low Power Design Methodologies

Jan M. Rabaey, Massoud Pedram



Low Power Design Methodologies:

Low Power Design Methodologies Jan M. Rabaey, Massoud Pedram, 2012-12-06 *Low Power Design Methodologies* presents the first in depth coverage of all the layers of the design hierarchy ranging from the technology circuit logic and architectural levels up to the system layer The book gives insight into the mechanisms of power dissipation in digital circuits and presents state of the art approaches to power reduction Finally it introduces a global view of low power design methodologies and how these are being captured in the latest design automation environments The individual chapters are written by the leading researchers in the area drawn from both industry and academia Extensive references are included at the end of each chapter Audience A broad introduction for anyone interested in low power design Can also be used as a text book for an advanced graduate class A starting point for any aspiring researcher

Introduction to Low-Power Design in VLSIs Patrick Lee, 2011-12-12 This book discusses one increasingly important issue in the VLSI design low power It covers the following topics a basic concepts of low power design b low power design methods and applications in industry chips and c commercial CAD tools on low power design This book discusses the concepts a set of known methods industry cases and CAD tools on the low power design It is organized in four chapters and a glossary is provided at the end of the book

Low Power Design Essentials Jan Rabaey, 2009-04-21 *Low Power Design Essentials* contains all the topics of importance to the low power designer The book lays the foundation with background chapters entitled Advanced MOS Transistors and Their Models and Power Basics These chapters are followed by chapters on the design process including optimization architecture and algorithm level memory run time standby logic and standby memory Chapters on special topics are also included power management and modal design ultra low power and low power design methodology and flows The book concludes with a chapter on case studies as well as a chapter on Projection into the Future These chapters are all based on the extensive amount of teaching that the author has carried out both at universities and companies worldwide All chapters have been drawn up specifically for self study They aim however at different levels of understanding All the chapters start with elementary material but most also contain advanced material

Low-Power Design Techniques and CAD Tools for Analog and RF Integrated Circuits Piet Wambacq, Georges Gielen, John Gerrits, 2007-05-08 This unique book provides an overview of the current state of the art and very recent research results that have been achieved as part of the Low Power Initiative of the European Union in the field of analogue RF and mixed signal design methodologies and CAD tools

Power Aware Design Methodologies Massoud Pedram, Jan M. Rabaey, 2007-05-08 *Power Aware Design Methodologies* was conceived as an effort to bring all aspects of power aware design methodologies together in a single document It covers several layers of the design hierarchy from technology circuit logic and architectural levels up to the system layer It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits digital and analog systems on chip microelectronic systems wirelessly networked systems of computational nodes and so on In addition to providing an

in depth analysis of the sources of power dissipation in VLSI circuits and systems and the technology and design trends this book provides a myriad of state of the art approaches to power optimization and control The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas Contributions are from both academia and industry The contributors have reported the various technologies methodologies and techniques in such a way that they are understandable and useful

Low Power Design in Deep Submicron Electronics W. Nebel, Jean Mermet, 2013-06-29 Low Power Design in Deep Submicron Electronics deals with the different aspects of low power design for deep submicron electronics at all levels of abstraction from system level to circuit level and technology Its objective is to guide industrial and academic engineers and researchers in the selection of methods technologies and tools and to provide a baseline for further developments Furthermore the book has been written to serve as a textbook for postgraduate student courses In order to achieve both goals it is structured into different chapters each of which addresses a different phase of the design a particular level of abstraction a unique design style or technology These design related chapters are amended by motivations in Chapter 2 which presents visions both of future low power applications and technology advancements and by some advanced case studies in Chapter 9 From the Foreword This global nature of design for low power was well understood by Wolfgang Nebel and Jean Mermet when organizing the NATO workshop which is the origin of the book They invited the best experts in the field to cover all aspects of low power design As a result the chapters in this book are covering deep submicron CMOS digital system design for low power in a systematic way from process technology all the way up to software design and embedded software systems Low Power Design in Deep Submicron Electronics is an excellent guide for the practicing engineer the researcher and the student interested in this crucial aspect of actual CMOS design It contains about a thousand references to all aspects of the recent five years of feverish activity in this exciting aspect of design Hugo de Man Professor K U Leuven Belgium Senior Research Fellow IMEC Belgium

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis Sumit Ahuja, Avinash Lakshminarayana, Sandeep Kumar Shukla, 2011-10-22 This book presents novel research techniques algorithms methodologies and experimental results for high level power estimation and power aware high level synthesis Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low power ASIC FPGA design

Practical Low Power Digital VLSI Design Gary K. Yeap, 2012-12-06 Practical Low Power Digital VLSI Design emphasizes the optimization and trade off techniques that involve power dissipation in the hope that the readers are better prepared the next time they are presented with a low power design problem The book highlights the basic principles methodologies and techniques that are common to most CMOS digital designs The advantages and disadvantages of a particular low power technique are discussed Besides the classical area performance trade off the impact to design cycle time complexity risk testability and reusability are discussed The wide impacts to all aspects of design are what make low power problems challenging and interesting Heavy emphasis is given to top down structured design style

with occasional coverage in the semicustom design methodology The examples and design techniques cited have been known to be applied to production scale designs or laboratory settings The goal of Practical Low Power Digital VLSI Design is to permit the readers to practice the low power techniques using current generation design style and process technology Practical Low Power Digital VLSI Design considers a wide range of design abstraction levels spanning circuit logic architecture and system Substantial basic knowledge is provided for qualitative and quantitative analysis at the different design abstraction levels Low power techniques are presented at the circuit logic architecture and system levels Special techniques that are specific to some key areas of digital chip design are discussed as well as some of the low power techniques that are just appearing on the horizon Practical Low Power Digital VLSI Design will be of benefit to VLSI design engineers and students who have a fundamental knowledge of CMOS digital design *Nano-CMOS Circuit and Physical Design* Ban Wong, Anurag Mittal, Yu Cao, Greg W. Starr, 2005-04-08 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation *SOC Design Methodologies* Michel Robert, Bruno Rouzeyre, Christian Pigué, Marie-Lise Flottes, 2013-03-15 The 11 th IFIP International Conference on Very Large Scale Integration in Montpellier France December 3 5 2001 was a great success The main focus was about IP Cores Circuits and System Designs 55 years ago in late 1947 the transistor was invented and everybody knows that it was by William Shockley John Bardeen and Walter H Brattain Bell Telephone Laboratories which received the Nobel Prize in Physics in 1956 Probably everybody thinks that it was recognized immediately as a major invention

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