
LOW-ENERGY FPGAs

Architecture and Design

by
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Kluwer Academic Publishers

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Guy Lemieux, David Lewis



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Low-Energy FPGAs — Architecture and Design Varghese George, Jan M. Rabaey, 2001-06-30 Low Energy FPGAs Architecture and Design is a primary resource for both researchers and practicing engineers in the field of digital circuit design The book addresses the energy consumption of Field Programmable Gate Arrays FPGAs FPGAs are becoming popular as embedded components in computing platforms The programmability of the FPGA can be used to customize implementations of functions on an application basis This leads to performance gains and enables reuse of expensive silicon Chapter 1 provides an overview of digital circuit design and FPGAs Chapter 2 looks at the implication of deep submicron technology on FPGA power dissipation Chapter 3 describes the exploration environment to guide and evaluate design decisions Chapter 4 discusses the architectural optimization process to evaluate the trade offs between the flexibility of the architecture and the effect on the performance metrics Chapter 5 reviews different circuit techniques to reduce the performance overhead of some of the dominant components Chapter 6 shows methods to configure FPGAs to minimize the programming overhead Chapter 7 addresses the physical realization of some of the critical components and the final implementation of a specific low energy FPGA Chapter 8 compares the prototype array to an equivalent commercial architecture

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FPGA Design Automation Deming Chen, Jason Cong, Peichen Pan, 2006 FPGA Design Automation A Survey is an up to date comprehensive survey tutorial of FPGA design automation with an emphasis on the recent developments within the past 5 to 10 years The focus is on the theory and techniques that have been or most likely will be reduced to practice It covers all major steps in FPGA design flow routing and placement circuit clustering technology mapping and architecture specific optimization physical synthesis RT level and behavior level synthesis and power optimization FPGA Design

Automation A Survey can be used as both a guide for beginners who are embarking on research in this relatively young yet exciting area and a useful reference for established researchers in this field

Design of Interconnection Networks for Programmable Logic Guy Lemieux, David Lewis, 2013-06-29 Programmable Logic Devices PLDs have become the key implementation medium for the vast majority of digital circuits designed today While the highest volume devices are still built with full fabrication rather than field programmability the trend towards ever fewer ASICs and more FPGAs is clear This makes the field of PLD architecture ever more important as there is stronger demand for faster smaller cheaper and lower power programmable logic PLDs are 90% routing and 10% logic This book focuses on that 90% that is the programmable routing the manner in which the programmable wires are connected and the circuit design of the programmable switches themselves Anyone seeking to understand the design of an FPGA needs to become literate in the complexities of programmable routing architecture This book builds on the state of the art of programmable interconnect by providing new methods of investigating and measuring interconnect structures as well as new programmable switch basic circuits The early portion of this book provides an excellent survey of interconnection structures and circuits as they exist today Lemieux and Lewis then provide a new way to design sparse crossbars as they are used in PLDs and show that the method works with an empirical validation This is one of a few routing architecture works that employ analytical methods to deal with the routing architecture design The analysis permits interesting insights not typically possible with the standard empirical approach

Reconfigurable Computing: Architectures, Tools and Applications Pedro C. Diniz, 2007-03-19 This book constitutes the refereed proceedings of the Third International Workshop on Applied Reconfigurable Computing ARC 2007 held in Mangaratiba Brazil in March 2007 The 27 full papers and 10 short papers presented together with a late comer contribution from ARC 2006 are organized in topical sections on architectures mapping techniques and tools arithmetic and applications

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Johan Vounckx, Nadine Azemard, 2006-09-08 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more

Fine- and Coarse-Grain Reconfigurable Computing Stamatis Vassiliadis, Dimitrios Soudris, 2007-10-12 Fine and Coarse Grain Reconfigurable Computing gives the basic concepts and building blocks for the design of Fine or FPGA and Coarse Grain Reconfigurable Architectures Recently developed integrated architecture design and software supported design flow of FPGA and coarse grain reconfigurable architecture are also described Part I consists of two extensive surveys of FPGA and Coarse Grain Reconfigurable Architectures The FPGA technology is defined which includes architecture logic block structure interconnect and configuration methods and existing fine grain reconfigurable

architectures emerged from both academia and industry. Additionally, the implementation techniques and CAD tools developed to facilitate the implementation of a system in reconfigurable hardware by the industry and academia are provided. In addition, the features, advantages, and limitations of the coarse grain reconfigurable systems, the specific issues that should be addressed during the design phase, as well as representative existing coarse grain reconfigurable systems are explained. In Part II, case studies, innovative research results about reconfigurable architectures and design frameworks from three projects: AMDREL, MOLEN, and ADRES DRESC, and a new classification according to microcoded architectural criteria are described. Fine and Coarse Grain Reconfigurable Computing is an essential reference for researchers and professionals and can be used as a textbook by undergraduate, graduate students, and professors. Foreword by Yale Patt, Jim Smith, and Mateo Valero.

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Vassilis Paliouras, Johan Vounckx, Diederik Verkest, 2005-08-25. Welcome to the proceedings of PATMOS 2005, the 15th in a series of international workshops. PATMOS 2005 was organized by IMEC with technical co-sponsorship from the IEEE Circuits and Systems Society. Over the years, PATMOS has evolved into an important European event where researchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design methodologies, and tools required for the development of upcoming generations of integrated circuits and systems. The technical program of PATMOS 2005 contained state-of-the-art technical contributions: three invited talks, a special session on hearing aid design, and an embedded tutorial. The technical program focused on timing, performance, and power consumption, as well as architectural aspects, with particular emphasis on modeling, design characterization, analysis, and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 74 papers to be presented at PATMOS. The papers were divided into 11 technical sessions and 3 poster sessions. As is always the case with the PATMOS workshops, the review process was anonymous; full papers were required, and several reviews were carried out per paper. Beyond the presentations of the papers, the PATMOS technical program was enriched by a series of speeches offered by world-class experts on important emerging research issues of industrial relevance. Prof. Jan Rabaey (Berkeley, USA) gave a talk on "Traveling the Wild Frontier of Ultra-Low Power Design." Dr. Sung Bae Park (Sung) gave a presentation on "DVL: Deep Low Voltage Circuits and Devices." Prof. Embedded Computer Systems: Architectures, Modeling, and Simulation Mladen Berekovic, Nikitas Dimopoulos, Stephan Wong, 2008-07-07. This book constitutes the refereed proceedings of the 8th International Workshop on Systems Architectures, Modeling, and Simulation (SAMOS 2008) held in Samos, Greece, in July 2008. The 24 revised full papers presented together with a contemplative keynote and additional papers of two special workshop sessions were carefully reviewed and selected from 62 submissions. The papers are organized in topical sections on: architecture, new frontiers, SoC, application-specific contributions, system-level design for heterogeneous systems, programming multicores, sensors and sensor networks, and systems modeling and design. Tree-based Heterogeneous

FPGA Architectures Umer Farooq,Zied Marrakchi,Habib Mehrez,2012-05-17 This book presents a new FPGA architecture known as tree based FPGA architecture due to its hierarchical nature This type of architecture has been relatively unexplored despite their better performance and predictable routing behavior as compared to mesh based FPGA architectures In this book we explore and optimize the tree based architecture and we evaluate it by comparing it to equivalent mesh based FPGA architectures

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