Background - Rapid IO



- Three-layered, embedded system interconnect architecture
 - Logical memory mapped I/O, message passing, and global shared memory
 - Transport routing based on packet destination ID
 - Physical serial and 8- or 16-bit parallel at 250, 500, or 1000 MHz
- Point-to-point, packet-switched interconnect
- Targeted for inter-processor and inter-board embedded interconnects
- Peak single-link throughput ranging from 2 to 64 Gb/s
- Focus on 16-bit parallel LVDS RIO implementation for satellite systems

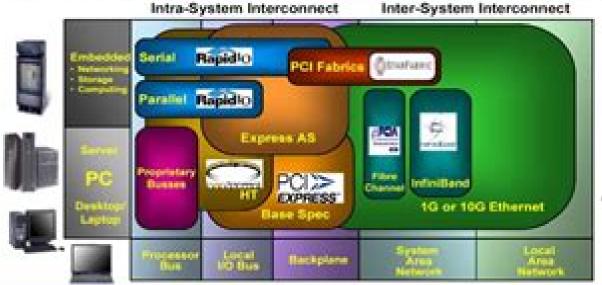


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Rapidio The Embedded System Interconnect

Sam Fuller

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