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Proceedings 2000 International Conference on Computer Design, 2000 **Energy Efficient Computing &** Electronics Santosh K. Kurinec, Sumeet Walia, 2019-01-31 In our abundant computing infrastructure performance improvements across most all application spaces are now severely limited by the energy dissipation involved in processing storing and moving data The exponential increase in the volume of data to be handled by our computational infrastructure is driven in large part by unstructured data from countless sources This book explores revolutionary device concepts associated circuits and architectures that will greatly extend the practical engineering limits of energy efficient computation from device to circuit to system level With chapters written by international experts in their corresponding field the text investigates new approaches to lower energy requirements in computing Features Has a comprehensive coverage of various technologies Written by international experts in their corresponding field Covers revolutionary concepts at the device circuit and system levels 2000 IEEE International Conference on Computer Design ,2000 **Artificial Intelligence Paradigms for** Smart Cyber-Physical Systems Luhach, Ashish Kumar, Elçi, Atilla, 2020-11-13 Cyber physical systems CPS have emerged as a unifying name for systems where cyber parts i e the computing and communication parts and physical parts are tightly integrated both in design and during operation Such systems use computations and communication deeply embedded in and interacting with human physical processes as well as augmenting existing and adding new capabilities As such CPS is an integration of computation networking and physical processes Embedded computers and networks monitor and control the physical processes with feedback loops where physical processes affect computations and vice versa The economic and societal potential of such systems is vastly greater than what has been realized and major investments are being made worldwide to develop the technology Artificial Intelligence Paradigms for Smart Cyber Physical Systems focuses on the recent advances in Artificial intelligence based approaches towards affecting secure cyber physical systems This book presents investigations on state of the art research issues applications and achievements in the field of computational intelligence paradigms for CPS Covering topics that include autonomous systems access control machine learning and intrusion detection and prevention systems this book is ideally designed for engineers industry professionals practitioners scientists managers students academicians and researchers seeking current research on artificial intelligence and cyber Electronic Design Automation for IC System Design, Verification, and Testing Luciano physical systems Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware

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elderly is presented with different techniques for the mobile ubiquitous and virtual environments System-on-Chip Bashir M. Al-Hashimi,2006-01-31 This book highlights both the key achievements of electronic systems design targeting SoC implementation style and the future challenges presented by the continuing scaling of CMOS technology

High-Performance Embedded Computing Marilyn Wolf, 2014-03-17 High Performance Embedded Computing Second Edition combines leading edge research with practical guidance in a variety of embedded computing topics including real time systems computer architecture and low power design Author Marilyn Wolf presents a comprehensive survey of the state of the art and guides you to achieve high levels of performance from the embedded systems that bring these technologies together The book covers CPU design operating systems multiprocessor programs and architectures and much more Embedded computing is a key component of cyber physical systems which combine physical devices with computational resources for control and communication This revised edition adds new content and examples of cyber physical systems throughout the book including design methodologies scheduling and wide area CPS to illustrate the possibilities of these new systems Revised and updated with coverage of recently developed consumer electronics architectures and models of computing Includes new VLIW processors such as the TI Da Vinci and CPU simulation Learn model based verification and middleware for embedded systems Supplemental material includes lecture slides labs and additional resources The Unknown Component Problem Tiziano Villa, Nina Yevtushenko, Robert K. Brayton, Alan Mishchenko, Alexandre Petrenko, Alberto Sangiovanni-Vincentelli, 2011-11-16 The Problem of the Unknown Component Theory and Applications addresses the issue of designing a component that combined with a known part of a system conforms to an overall specification The authors tackle this problem by solving abstract equations over a language The most general solutions are studied when both synchronous and parallel composition operators are used. The abstract equations are specialized to languages associated with important classes of automata used for modeling systems The book is a blend of theory and practice which includes a description of a software package with applications to sequential synthesis of finite state machines Specific topologies interconnecting the components exact and heuristic techniques and optimization scenarios are studied Finally the scope is enlarged to domains like testing supervisory control game theory and synthesis for special omega languages The authors present original results of the authors along with an overview of existing ones Low-Power High-Level Synthesis for Nanoscale CMOS Circuits Saraju P. Mohanty, Nagarajan Ranganathan, Elias Kougianos, Priyardarsan Patra, 2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor

is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation. The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits Compact Models and Performance Investigations for Subthreshold Interconnects Rohit Dhiman, Rajeevan Chandel, 2014-11-07 The book provides a detailed analysis of issues related to sub threshold interconnect performance from the perspective of analytical approach and design techniques Particular emphasis is laid on the performance analysis of coupling noise and variability issues in sub threshold domain to develop efficient compact models The proposed analytical approach gives physical insight of the parameters affecting the transient behavior of coupled interconnects Remedial design techniques are also suggested to mitigate the effect of coupling noise The effects of wire width spacing between the wires wire length are thoroughly investigated In addition the effect of parameters like driver strength on peak coupling noise has also been analyzed Process voltage and temperature variations are prominent factors affecting sub threshold design and have also been investigated The process variability analysis has been carried out using parametric analysis process corner analysis and Monte Carlo technique The book also provides a qualitative summary of the work reported in the literature by various researchers in the design of digital sub threshold circuits This book should be of interest for researchers and graduate students with deeper insights into sub threshold interconnect models in particular In this sense this book will best fit as a text book and or a reference book for students who are initiated in the area of research and advanced courses in nanotechnology interconnect design and modeling

Artificial Intelligence in Design '02 Asko Riitahuhta,2002-07-31 One of the foundations for change in our society comes from designing Its genesis is the notion that the world around us either is unsuited to our needs or can be improved. The need for designing is driven by a society s view that it can improve or add value to human existence well beyond simple subsistence As a consequence of designing the world which we inhabit is increasingly a designed rather than a naturally occurring one In that sense it is an artificial world Designing is a fundamental precursor to manufacturing fabrication construction or implementation Design research aims to develop an understanding of designing and to produce models of designing that can be used to aid designing Artificial intelligence has provided an environmental paradigm within which

design research based on computational constructions can be carried out Design research can be carried out in variety of ways It can be viewed as largely an empirical endeavour in which experiments are designed and executed in order to test some hypothesis about some design phenomenon or design behaviour This is the approach adopted in cognitive science It often manifests itself through the use of protocol studies of designers The results of such research form the basis of a computational model A second view is that design research can be carried out by positing axioms and then deriving Modeling, Analysis and Optimization of Network-on-Chip Communication consequences from them Architectures Umit Y. Ogras, Radu Marculescu, 2013-03-12 Traditionally design space exploration for Systems on Chip SoCs has focused on the computational aspects of the problem at hand However as the number of components on a single chip and their performance continue to increase the communication architecture plays a major role in the area performance and energy consumption of the overall system As a result a shift from computation based to communication based design becomes mandatory Towards this end network on chip NoC communication architectures have emerged recently as a promising alternative to classical bus and point to point communication architectures In this dissertation we study outstanding research problems related to modeling analysis and optimization of NoC communication architectures More precisely we present novel design methodologies software tools and FPGA prototypes to aid the design of application specific **Handbook of Computer Architecture** Anupam Chattopadhyay, 2024-12-20 This handbook presents the key topics NoCs in the area of computer architecture covering from the basic to the most advanced topics including software and hardware design methodologies It will provide readers with the most comprehensive updated reference information covering applications in single core processors multicore processors application specific processors reconfigurable architectures emerging computing architectures processor design and programming flows test and verification This information benefits the readers as a full and quick technical reference with a high level review of computer architecture technology detailed iRODS Primer 2 Yu-Ting Chen, Jason Cong, Michael Gill, Glenn technical descriptions and the latest practical applications Reinman, Bingjun Xiao, Zhiyang Ong, 2015-07-01 Since the end of Dennard scaling in the early 2000s improving the energy efficiency of computation has been the main concern of the research community and industry. The large energy efficiency gap between general purpose processors and application specific integrated circuits ASICs motivates the exploration of customizable architectures where one can adapt the architecture to the workload In this Synthesis lecture we present an overview and introduction of the recent developments on energy efficient customizable architectures including customizable cores and accelerators on chip memory customization and interconnect optimization. In addition to a discussion of the general techniques and classification of different approaches used in each area we also highlight and illustrate some of the most successful design examples in each category and discuss their impact on performance and energy efficiency. We hope that this work captures the state of the art research and development on customizable architectures and serves as a useful

reference basis for further research design and implementation for large scale deployment in future computing systems **Embedded Systems Handbook 2-Volume Set** Richard Zurawski, 2018-10-08 During the past few years there has been an dramatic upsurge in research and development implementations of new technologies and deployments of actual solutions and technologies in the diverse application areas of embedded systems. These areas include automotive electronics industrial automated systems and building automation and control Comprising 48 chapters and the contributions of 74 leading experts from industry and academia the Embedded Systems Handbook Second Edition presents a comprehensive view of embedded systems their design verification networking and applications. The contributors directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews exploring new developments deployments and trends To accommodate the tremendous growth in the field the handbook is now divided into two volumes New in This Edition Processors for embedded systems Processor centric architecture description languages Networked embedded systems in the automotive and industrial automation fields Wireless embedded systems Embedded Systems Design and Verification Volume I of the handbook is divided into three sections It begins with a brief introduction to embedded systems design and verification The book then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Networked Embedded Systems Volume II focuses on selected application areas of networked embedded systems It covers automotive field industrial automation building automation and wireless sensor networks This volume highlights implementations in fast evolving areas which have not received proper coverage in other publications Reflecting the unique functional requirements of different application areas the contributors discuss inter node communication aspects in the context of specific applications of networked embedded systems Handbook of Research on Mobility and Computing: Evolving Technologies and Ubiquitous Impacts Cruz-Cunha, Maria Manuela, Moreira, Fernando, 2011-04-30 Discusses the main issues challenges opportunities and trends related to this explosive range of new developments and applications in constant evolution and impacting every organization and society as a whole This two volume handbook supports post graduate students teachers and researchers as well as IT professionals and managers A Primer on Compression in the Memory Hierarchy Somayeh Sardashti, Angelos Arelakis, Per Stenström, David A. Wood, 2015-12-01 This synthesis lecture presents the current state of the art in applying low latency lossless hardware compression algorithms to cache memory and the memory cache link There are many non trivial challenges that must be addressed to make data compression work well in this context First since compressed data must be decompressed before it can be accessed decompression latency ends up on the critical memory access path This imposes a significant constraint on the choice of compression algorithms Second while conventional memory systems store fixed size entities like data types cache blocks and memory pages these entities will suddenly vary in

size in a memory system that employs compression Dealing with variable size entities in a memory system using compression has a significant impact on the way caches are organized and how to manage the resources in main memory We systematically discuss solutions in the open literature to these problems Chapter 2 provides the foundations of data compression by first introducing the fundamental concept of value locality We then introduce a taxonomy of compression algorithms and show how previously proposed algorithms fit within that logical framework Chapter 3 discusses the different ways that cache memory systems can employ compression focusing on the trade offs between latency capacity and complexity of alternative ways to compact compressed cache blocks Chapter 4 discusses issues in applying data compression to main memory and Chapter 5 covers techniques for compressing data on the cache to memory links This book should help a skilled memory system designer understand the fundamental challenges in applying compression to the memory hierarchy and introduce him her to the state of the art techniques in addressing them

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