

Functional Verification Methodology for the PowerPC 604™ Microprocessor

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Abstract

Functional (i.e., logic) verification of the current generation of complex, super-scalar microprocessors such as the PowerPC 604™ microprocessor presents significant challenges to a project's verification participants. Simple architectural level tests are insufficient to gain confidence in the quality of the design. Detailed planning must be combined with a broad collection of methods and tools to ensure that design defects are detected as early as possible in a project's life-cycle.

This paper discusses the methodology applied to the functional verification of the PowerPC 604 microprocessor.

1. Introduction

Only in recent years have industry practitioners begun publishing information detailing functional verification practices and procedures [1, 2, & 3]. Building on work previously published describing the PowerPC 604 microprocessor project [4 & 5], this paper describes the functional verification methodology employed. The design methodology and specification approach are briefly discussed. Practices covering project and verification planning, testcase generation, simulation, coverage assessment, and design quality confidence are included. Finally, possibilities for future improvements to these functional verification practices are examined.

The term "verification methodology" used in this paper should be interpreted to mean "an integrated set of techniques and methods applied to produce a defect-free microprocessor design".

2. Design Methodology and Specification Approach

At the Somerset Design Center, methods and tools used in the microprocessor verification effort are significantly influenced by the tools used to develop the design model.

2.1 Development and Design Modeling

The selected hardware design modeling language (HDL) now entrenched in the design process is a proprietary superset of the Verilog language. Depending upon how a design is partitioned, portions of the logic and physical design may be synthesized while other portions may be constructed as custom logic and layout in a traditional manner. The logical and physical design characteristics can then be analyzed in parallel.

The design's logic characteristics are examined from the perspective of functional logic -- "Does the design correctly execute according to the architectural and implementation-dependent design specifications?". For the PowerPC 604 microprocessor project, design description was captured at the gate and logic device levels. Using a variety of tools for compilation and translation, models were produced in forms usable by multiple simulation systems including a Verilog event-driven simulator and proprietary cycle based simulators. Simulation was performed to verify the correctness of the simulation model.

The design's physical characteristics were examined from the perspective of physical circuit design -- "Does the design correctly meet desired timing and electronic specifications (i.e., set-up and hold constraints, switching speeds, power consumption, etc.)".

An equivalency check, shown in Figure 1, was performed periodically to ensure that the hardware technology description of the design was synchronized with the high-level logical description.

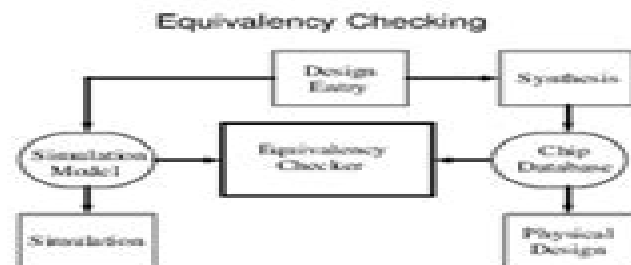


Figure 1: Equivalency Check and Logical/Physical Views

Figure 2 illustrates the design process used by the PowerPC 604 microprocessor project. It resembled a spiral-type software development approach. Most project effort involved two (iterative) steps:

- improve design, and
- evaluate improvements;

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Table of Contents Proceedings 1996 33rd Design Automation Conference

1. Understanding the eBook Proceedings 1996 33rd Design Automation Conference
 - The Rise of Digital Reading Proceedings 1996 33rd Design Automation Conference
 - Advantages of eBooks Over Traditional Books
2. Identifying Proceedings 1996 33rd Design Automation Conference
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Proceedings 1996 33rd Design Automation Conference
 - User-Friendly Interface
4. Exploring eBook Recommendations from Proceedings 1996 33rd Design Automation Conference
 - Personalized Recommendations
 - Proceedings 1996 33rd Design Automation Conference User Reviews and Ratings

- Proceedings 1996 33rd Design Automation Conference and Bestseller Lists
- 5. Accessing Proceedings 1996 33rd Design Automation Conference Free and Paid eBooks
 - Proceedings 1996 33rd Design Automation Conference Public Domain eBooks
 - Proceedings 1996 33rd Design Automation Conference eBook Subscription Services
 - Proceedings 1996 33rd Design Automation Conference Budget-Friendly Options
- 6. Navigating Proceedings 1996 33rd Design Automation Conference eBook Formats
 - ePub, PDF, MOBI, and More
 - Proceedings 1996 33rd Design Automation Conference Compatibility with Devices
 - Proceedings 1996 33rd Design Automation Conference Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Proceedings 1996 33rd Design Automation Conference
 - Highlighting and Note-Taking Proceedings 1996 33rd Design Automation Conference
 - Interactive Elements Proceedings 1996 33rd Design Automation Conference
- 8. Staying Engaged with Proceedings 1996 33rd Design Automation Conference
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Proceedings 1996 33rd Design Automation Conference
- 9. Balancing eBooks and Physical Books Proceedings 1996 33rd Design Automation Conference
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Proceedings 1996 33rd Design Automation Conference
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Proceedings 1996 33rd Design Automation Conference
 - Setting Reading Goals Proceedings 1996 33rd Design Automation Conference
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Proceedings 1996 33rd Design Automation Conference
 - Fact-Checking eBook Content of Proceedings 1996 33rd Design Automation Conference
 - Distinguishing Credible Sources

13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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