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Eugenio Villar Bonet



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Proceedings, International Test Conference 1997, 1997 **Proceedings**, 1998 *Proceedings International Test Conference 1998 (IEEE Cat. No.98CH36270)*, 1998 Index of Conference Proceedings British Library. Document Supply Centre, 1999 **The Boundary — Scan Handbook** Kenneth P. Parker, 2012-12-06 In February of 1990 the balloting process for the IEEE proposed standard P1149 1 was completed creating IEEE Std 1149 1 1990 Later that summer in record time the standard won ratification as an ANSI standard as well This completed over six years of intensive cooperative effort by a diverse group of people who share a vision on solving some of the severe testing problems that exist now and are steadily getting worse Early in this process someone asked me if I thought that the P1149 1 effort would ever bear fruit I responded somewhat glibly that it was anyone's guess Well it wasn't anyone's guess but rather the faith of a few individuals in the proposition that many testing problems could be solved if a multifaceted industry could agree on a standard for all to follow Four of these individuals stand out they are Harry Bleeker Colin Maunder Rodham Tulloss and Lee Whetsel In that I am convinced that the 1149 1 standard is the most significant testing development in the last 20 years I personally feel a debt of gratitude to them and all the people who labored on the various Working Groups in its creation *Fault Diagnosis of Analog Integrated Circuits* Prithviraj Kabisatpathy, Alok Barua, Satyabroto Sinha, 2006-01-13 System on Chip SOC having both digital and analog circuits has become increasingly prevalent in integrated circuit manufacturing industry Electronic tests are classified as digital analog and mixed signal Current methodologies for the testing of digital circuits are well developed In contrast methodologies for the testing of analog circuits remain relatively underdeveloped due to the complex nature of analog signals Compared to digital testing analog testing lags far behind in methodologies and tools and therefore demands substantial research and development effort Fault Diagnosis of Analog Integrated Circuits is a textbook for advanced undergraduate and graduate level students as well as practicing engineers The objective of this book is to study the testing and fault diagnosis of analog and analog part of mixed signal circuits A background in analog integrated circuit artificial neural network is desirable but not essential The text covers the testing and fault diagnosis of both bipolar and Metal Oxide Semiconductor MOS circuits Fault model of the devices in analog domain has been introduced in the text The test stimulus generations are also discussed in details Experimental verification of some state of the art techniques has also been presented in the book It also contains problems that can be used as quiz or homework This book enables the reader to test an analog circuit that is implemented either in bipolar or MOS technology **System-on-Chip** Bashir M. Al-Hashimi, 2006-01-31 This book highlights both the key achievements of electronic systems design targeting SoC implementation style and the future challenges presented by the continuing scaling of CMOS technology **Design and Test Technology for Dependable Systems-on-Chip** Ubar, Raimund, Raik, Jaan, Vierhaus, Heinrich Theodor, 2010-12-31 This book covers aspects of system design and efficient modelling and also introduces various fault models and fault

mechanisms associated with digital circuits integrated into System on Chip SoC Multi Processor System on Chip MPSoC or Network on Chip NoC

Data Mining and Diagnosing IC Fails Leendert M. Huisman, 2006-10-03 This book grew out of an attempt to describe a variety of tools that were developed over a period of years in IBM to analyze Integrated Circuit fail data The selection presented in this book focuses on those tools that have a significant statistical or datamining component The danger of describing statistical analysis methods is the amount of non trivial mathematics that is involved and that tends to obscure the usually straightforward analysis ideas This book is therefore divided into two roughly equal parts The first part contains the description of the various analysis techniques and focuses on ideas and experimental results The second part contains all the mathematical details that are necessary to prove the validity of the analysis techniques the existence of solutions to the problems that those techniques engender and the correctness of several properties that were assumed in the first part Those who are interested only in using the analysis techniques themselves can skip the second part but that part is important if only to understand what is being done

Multi-Core Embedded Systems Georgios Kornaros, 2018-10-08 Details a real world product that applies a cutting edge multi core architecture Increasingly demanding modern applications such as those used in telecommunications networking and real time processing of audio video and multimedia streams require multiple processors to achieve computational performance at the rate of a few giga operations per second This necessity for speed and manageable power consumption makes it likely that the next generation of embedded processing systems will include hundreds of cores while being increasingly programmable blending processors and configurable hardware in a power efficient manner Multi Core Embedded Systems presents a variety of perspectives that elucidate the technical challenges associated with such increased integration of homogeneous processors and heterogeneous multiple cores It offers an analysis that industry engineers and professionals will need to understand the physical details of both software and hardware in embedded architectures as well as their limitations and potential for future growth Discusses the available programming models spread across different abstraction levels The book begins with an overview of the evolution of multiprocessor architectures for embedded applications and discusses techniques for autonomous power management of system level parameters It addresses the use of existing open source and free tools originating from several application domains such as traffic modeling graph theory parallel computing and network simulation In addition the authors cover other important topics associated with multi core embedded systems such as Architectures and interconnects Embedded design methodologies Mapping of applications

Analog and Mixed-Signal Boundary-Scan Adam Osseiran, 2013-03-09 This book contains more than the IEEE Standard 1149 4 It also contains the thoughts of those who developed the standard Adam Osseiran has edited the original writings of Brian Wilkins Colin Maunder Rod Tulloss Steve Sunter Mani Soma Keith Lofstrom and John McDermid all of whom have personally contributed to this standard To preserve the original spirit only minor changes were made and the reader will sense a chapter to chapter variation in the style of expression This may appear awkward to some

although I found the lack of monotonicity refreshing A system consists of a specific organization of parts The function of the system cannot be performed by an individual part or even a disorganized collection of the same parts Testing has a system like characteristic Testing of a system does not follow directly from the testing of its parts and a system built with testable parts can sometimes be impossible to test Therefore testability of the system must be organized Some years ago the IEEE published the boundary scan Standard 1149.1 That Standard provided an architecture for digital VLSI chips The chips designed with the 1149.1 architecture can be integrated into a testable system However many systems today contain both analog and digital chips Even if all digital chips are compliant with the standard the testability of a mixed signal system cannot be guaranteed The new Standard 1149.4 described in this book extends the previous architecture to mixed signal systems

Dependable Multicore Architectures at Nanoscale Marco Ottavi, Dimitris Gizopoulos, Salvatore Pontarelli, 2017-08-28 This book provides comprehensive coverage of the dependability challenges in today's advanced computing systems It is an in depth discussion of all the technological and design level techniques that may be used to overcome these issues and analyzes various dependability assessment methods The impact of individual application scenarios on the definition of challenges and solutions is considered so that the designer can clearly assess the problems and adjust the solution based on the specifications in question The book is composed of three sections beginning with an introduction to current dependability challenges arising in complex computing systems implemented with nanoscale technologies and of the effect of the application scenario The second section details all the fault tolerance techniques that are applicable in the manufacture of reliable advanced computing devices Different levels from technology level fault avoidance to the use of error correcting codes and system level checkpointing are introduced and explained as applicable to the different application scenario requirements Finally the third section proposes a roadmap of future trends in and perspectives on the dependability and manufacturability of advanced computing systems from the special point of view of industrial stakeholders Dependable Multicore Architectures at Nanoscale showcases the original ideas and concepts introduced into the field of nanoscale manufacturing and systems reliability over nearly four years of work within COST Action IC1103 MEDIAN a think tank with participants from 27 countries Academic researchers and graduate students working in multi core computer systems and their manufacture will find this book of interest as will industrial design and manufacturing engineers working in VLSI companies

Soft Errors in Modern Electronic Systems Michael Nicolaidis, 2010-09-24 This book provides a comprehensive presentation of the most advanced research results and technological developments enabling understanding qualifying and mitigating the soft errors effect in advanced electronics including the fundamental physical mechanisms of radiation induced soft errors the various steps that lead to a system failure the modelling and simulation of soft error at various levels including physical electrical netlist event driven RTL and system level modelling and simulation hardware fault injection accelerated radiation testing and natural environment testing soft error oriented test structures process level device level cell level

circuit level architectural level software level and system level soft error mitigation techniques The book contains a comprehensive presentation of most recent advances on understanding qualifying and mitigating the soft error effect in advanced electronic systems presented by academia and industry experts in reliability fault tolerance EDA processor SoC and system design and in particular experts from industries that have faced the soft error impact in terms of product reliability and related business issues and were in the forefront of the countermeasures taken by these companies at multiple levels in order to mitigate the soft error effects at a cost acceptable for commercial products In a fast moving field where the impact on ground level electronics is very recent and its severity is steadily increasing at each new process node impacting one after another various industry sectors as an example the Automotive Electronics Council comes to publish qualification requirements on soft errors research and technology developments and industrial practices have evolve very fast outdated the most recent books edited at 2004

Design of Hardware/Software Embedded Systems Eugenio Villar Bonet,2001

Este libro presenta los desaf os planteados por las nuevas y sumamente poderosas tecnolog as de integraci n de sistemas electr nicos que est n en la base de los cambios sociales hacia lo que llaman la Sociedad de la Informaci n en la que los dispositivos electr nicos se har n una parte incorporada de la vida diaria encajados en casi cada producto Es necesario un conocimiento cuidadoso de los desaf os para aprovechar la amplia gama de ocasiones ofrecidas por tales capacidades de integraci n y las correspondientes posibilidades de dise o de sistemas electr nicos

Models in Hardware Testing

Hans-Joachim Wunderlich,2009-11-12 Model based testing is the most powerful technique for testing hardware and software systems Models in Hardware Testing describes the use of models at all the levels of hardware testing The relevant fault models for nanoscaled CMOS technology are introduced and their implications on fault simulation automatic test pattern generation fault diagnosis memory testing and power aware testing are discussed Models and the corresponding algorithms are considered with respect to the most recent state of the art and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance

Testing for Small-Delay Defects in Nanoscale CMOS

Integrated Circuits Sandeep K. Goel,Krishnendu Chakrabarty,2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs However the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations power supply noise crosstalk resistive opens bridges and design for manufacturing DfM related rule violations The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non critical paths in the circuit Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on alternative methods that explores new

metrics top off ATPG and circuit topology based solutions Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement Written from the triple viewpoint of university researchers EDA tool developers and chip designers and tool users this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective The book is designed as a one stop reference for current industrial practices research challenges in the domain of SDD testing and recent developments in SDD solutions

Building a Successful Board-Test Strategy Stephen Scheiber, 2001-10-12 Part I Strategies and Tactics Part II Making the Job Easier 7 Environmental Stress Screening Part III Creating Test Solutions Part IV Pulling It All Together Appendix

Low-Power High-Resolution Analog to Digital Converters Amir Zjajo, José Pineda de Gyvez, 2010-10-29 With the fast advancement of CMOS fabrication technology more and more signal processing functions are implemented in the digital domain for a lower cost lower power consumption higher yield and higher re configurability This has recently generated a great demand for low power low voltage A D converters that can be realized in a mainstream deep submicron CMOS technology However the discrepancies between lithography wavelengths and circuit feature sizes are increasing Lower power supply voltages significantly reduce noise margins and increase variations in process device and design parameters Consequently it is steadily more difficult to control the fabrication process precisely enough to maintain uniformity The inherent randomness of materials used in fabrication at nanoscopic scales means that performance will be increasingly variable not only from die to die but also within each individual die Parametric variability will be compounded by degradation in nanoscale integrated circuits resulting in instability of parameters over time eventually leading to the development of faults Process variation cannot be solved by improving manufacturing tolerances variability must be reduced by new device technology or managed by design in order for scaling to continue Similarly within die performance variation also imposes new challenges for test methods In an attempt to address these issues Low Power High Resolution Analog to Digital Converters specifically focus on i improving the power efficiency for the high speed and low spurious spectral A D conversion performance by exploring the potential of low voltage analog design and calibration techniques respectively and ii development of circuit techniques and algorithms to enhance testing and debugging potential to detect errors dynamically to isolate and confine faults and to recover errors continuously The feasibility of the described methods has been verified by measurements from the silicon prototypes fabricated in standard 180nm 90nm and 65nm CMOS technology

Oscillation-Based Test in Mixed-Signal Circuits Gloria Huertas Sánchez, Diego Vázquez García de la Vega, Adoración Rueda Rueda, Jose Luis Huertas Díaz, 2007-06-03 Oscillation Based Test in Mixed Signal Circuits presents the development and experimental validation of the structural test strategy called Oscillation Based Test OBT in short The results here presented allow to assert not only from a theoretical point of view but also based on a wide experimental support that OBT is an efficient defect oriented test solution complementing the existing functional test techniques for mixed signal circuits

Thermal Testing of Integrated Circuits J. Altet, Antonio

Rubio,2013-03-09 Integrated circuits IC s have undergone a significant evolution in terms of complexity and performance as a result of the substantial advances made in manufacturing technology Circuits in their various mixed formats can be made up tens or even hundreds of millions of devices They work at extremely low voltages and switch at very high frequencies Testing of circuits has become an essential process in IC manufacturing in the effort to ensure that the manufactured components have the appropriate levels of quality Along with the ongoing trend towards more advanced technology and circuit features major testing challenges are continuously emerging The use of ambivalent procedures to test the analogue and digital sections of such complex circuits without interfering in their nominal operation is clearly a critical part of today s technological ipdustries Chapter 1 presents the general purposes and basic concepts rel ted With thetesting of integrated circuits discussing the various strategies and their limitations Readers who are already familiar with the field may opt to skip this chapter This book offers a multidisciplinary focus on thermal testing This is a testing method which is not only suitable for use in combination with other existing techniques but is also backed by a wealth of knowledge and offers exciting opportunities in the form of as yet unexplored areas of research and innovation for industrial applications

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