

Coupled device, circuit and interconnect simulation

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Abstract:

In this paper, we discuss several aspects that are related to coupling device, circuit and interconnect simulation software. Straightforward co-simulation is too time-consuming, and hence reduced order modelling must be used in order to summarize the behaviour of individual simulations into compact models. From a theoretical point of view, the problem is complicated by the fact that equations of different type are being coupled. Mathematical techniques are indispensable for guaranteeing acceptable simulation times.

The European project CODESTAR aims at providing a framework in which the aforementioned coupled simulations can be performed. The examples given in this paper have been taken from that project.

1. Introduction

For the design of complex integrated systems, knowledge of the electromagnetic coupling in passive components like inductors, capacitors and critical parts of net lists are indispensable. Today's extraction software tools use the static approach to quantify this coupling, thereby ignoring the Maxwell or wave-dynamic aspect of electromagnetic radiation. Whereas such an approach is valid at moderate frequencies, high-frequency effects are a major design concern for the next generation of architectures. The International Technology Roadmap for Semiconductors recognizes the lack of appropriate future design tools. In particular design tools that include high frequency effects are a difficult challenge for a successful implementation of the 65 nm node corresponding to circuit frequencies exceeding 5 GHz. The effects are physically understood, but TCAD software programs that can deal with them are not available. Figure 1 (inspired by [6]) summarizes the effects that play a role in the analysis of passive structures: electric and magnetic coupling of segments through air and oxide, current crowding at edges due to the skin effect and eddy currents, proximity effects due to presence of nearby segments, radiation, substrate injection, and substrate current caused by ohmic, eddy and displacement currents.

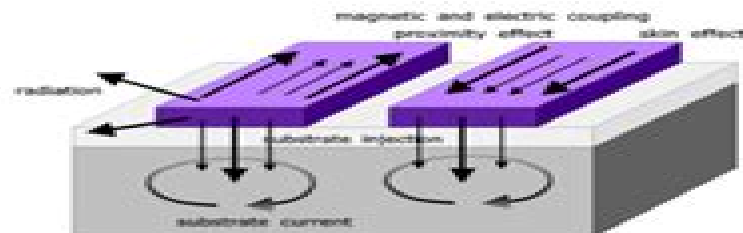


Figure 1. Summary of effects occurring in passive structures.

To accelerate the design of high-frequency passive on-chip structures and interconnects, the development of new modelling algorithms is needed. This task is addressed in the CODESTAR project. The resulting software will be used in a design cycle, starting from standardized geometrical data (GDS II format), and returning as output a manageable simulation net list that can be coupled to a network simulator such as SPICE or Pstar.

The situation becomes even more complicated when substrate noise analysis is required. As feature sizes decrease, substrate coupling noise may cause design failures and poor yields due to injected currents disturbing the operation of sensitive components. Any design targeted at sub-quarter micron process technologies may be vulnerable to substrate parasitics. Rule of thumb methodologies may turn out to be inadequate or lead to over-engineered designs. Reliable results can only be obtained by taking into account semiconductor physics. Tools like SubstrateStorm from Cadence perform such analyses by supplying RC net lists and reduced RC net lists, which can be coupled to network simulators. More accurate results are obtained when drift-diffusion models of semiconductor devices are used. In section 3 an example is given discussing precisely this topic, showing that it is indeed possible to couple device, circuit and interconnect simulations to obtain reliable models for substrate coupling noise.

Principles Of Circuit And Interconnect Simulation

Mei Song Tong, Xiao Yu Li



Principles Of Circuit And Interconnect Simulation:

Circuit Simulation Principles and Techniques and Their Application Toward Interconnect Simulation Kirk Alan Ingemunson, 1994 **Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation** Rene van Leuken, Gilles Sicard, 2011-02-04 This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble France in September 2010 The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows circuit techniques low power circuits self timed circuits process variation high level modeling of poweraware heterogeneous designs in SystemC AMS and minalogic **Coupled Multiscale Simulation and Optimization in Nanoelectronics** Michael Günther, 2015-06-15 Designing complex integrated circuits relies heavily on mathematical methods and calls for suitable simulation and optimization tools The current design approach involves simulations and optimizations in different physical domains device circuit thermal electromagnetic and in a range of electrical engineering disciplines logic timing power crosstalk signal integrity system functionality COMSON was a Marie Curie Research Training Network created to meet these new scientific and training challenges by a developing new descriptive models that take these mutual dependencies into account b combining these models with existing circuit descriptions in new simulation strategies and c developing new optimization techniques that will accommodate new designs The book presents the main project results in the fields of PDAE modeling and simulation model order reduction techniques and optimization based on merging the know how of three major European semiconductor companies with the combined expertise of university groups specialized in developing suitable mathematical models numerical schemes and e learning facilities In addition a common Demonstrator Platform for testing mathematical methods and approaches was created to assess whether they are capable of addressing the industry s problems and to educate young researchers by providing hands on experience with state of the art problems **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** Johan Vounckx, Nadine Azemard, 2006-09-08 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more **Proceedings of the Fourth International Symposium of Process Physics and Modeling in Semiconductor Technology** G. R. Srinivasan, C. S. Murthy, Scott T. Dunham, 1996 **Analytical Methodology of Tree Microstrip Interconnects Modelling For Signal Distribution** Blaise Ravelo, 2019-11-21 This book focuses on the modelling methodology of microstrip interconnects discussing various structures of single input multiple output SIMO tree interconnects for signal integrity SI engineering

Further it describes lumped and distributed transmission line elements based on single input single output SIMO models of symmetric and asymmetric trees and investigates more complicated phenomenon such as interbranch coupling The modelling approaches are based on the analytical methods using the Z Y and T matrices The established method enables the S parameters and voltage transfer function of SIMO tree to be determined Providing illustrative results with frequency and time domain analyses for each tree interconnect structure the book is a valuable resource for researchers engineers and graduate students in fields of analogue RF microwave digital and mixed circuit design SI and manufacturing engineering

Co-simulations of Microwave Circuits and High-Frequency Electromagnetic Fields Mei Song Tong,Xiao Yu Li,2024-07-03

This book aims to provide many advanced application topics for microwave circuits and high frequency electromagnetic EM fields by using advanced design system ADS and high frequency structure simulator HFSS as simulation platforms In particular it contains the latest multidisciplinary co simulation guidance on the design of relevant components and devices Currently the circuit field design and performance analysis and optimization strongly rely on various kinds of robust electronic design automation EDA software RF microwave engineers must grasp two or more types of related simulation design software ADS by Keysight and HFSS by Ansys are the representative for circuit simulations and for field and structural simulations of microwave devices respectively At present these two types of software are widely used in enterprises universities and research institutions The main purpose of this book is to enable readers who are interested in microwave engineering and applied electromagnetics to master the applications of these two tools It also helps readers expand their knowledge boundaries behind those types of software and deepen their understanding of developing interdisciplinary technologies by co simulations The book is divided into three parts The first part introduces the two latest versions of ADS and HFSS and helps readers better understand the basic principles and latest functions better It also advises how to choose appropriate simulation tools for different problems The second part mainly describes co simulations for high frequency EM fields microwave circuits antenna designs EM compatibility EMC and thermal and structural analyses It provides guides and advices on performing co simulations by ADS and HFSS incorporated with other types of software respectively The last part narrates the automation interfaces and script programming methods for co simulations It primarily deals with the Advanced Extension Language AEL Python Data Link PDL and MATLAB interface in ADS For HFSS it discusses VBScript IronPython scripting and Application Programming Interface APIs based on MATLAB Each topic contains practical examples to help readers understand so that they can gain a solid knowledge and skills regarding automated interfaces and scripting methods based on these kinds of software Concisely written in combination with practical examples this book is very suitable as a textbook in introductory courses on microwave circuit and EM simulations and also as a supplementary textbook in many courses on electronics microwave engineering communication engineering and related fields As well it can serve as a reference book for microwave engineers and researchers Integrated Circuit and System

Design, Power and Timing Modeling, Optimization and Simulation Nadine Azemard, Lars Svensson, 2007-08-21 This volume features the refereed proceedings of the 17th International Workshop on Power and Timing Modeling Optimization and Simulation Papers cover high level design low power design techniques low power analog circuits statistical static timing analysis power modeling and optimization low power routing optimization security and asynchronous design low power applications modeling and optimization and more

High-Speed Interconnects in VLSI Design, Modeling, and Signal Integrity Dr. Bhaskar Gugulothu, The rapid advancement in VLSI Very Large Scale Integration technology has ushered in a new era of high performance systems where interconnects have become a critical bottleneck in determining speed power and reliability This textbook provides a comprehensive understanding of high speed interconnect design analytical and simulation based modeling techniques and signal integrity challenges in modern integrated circuits It is intended for graduate students researchers and industry professionals involved in IC design and signal integrity analysis

Circuit-Technology

Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM

subarray design in deeply scaled nodes

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