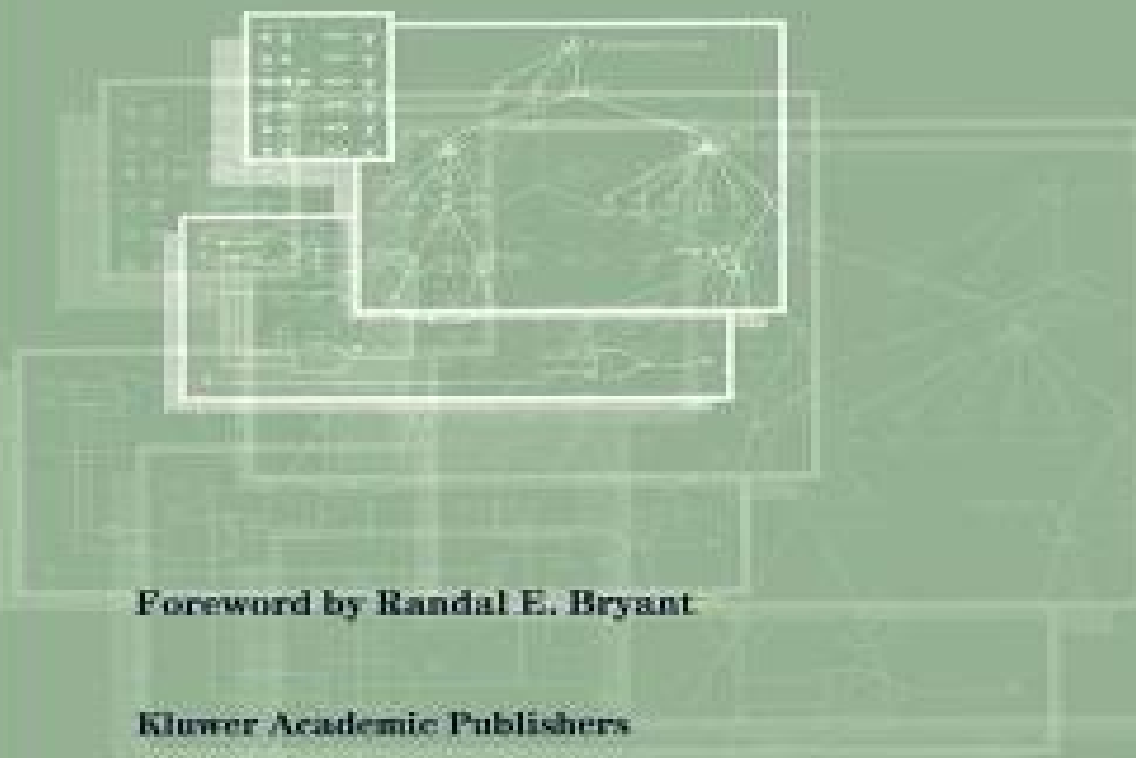Wolfgang Kunz and Dominik Stoffel

# Reasoning in Boolean Networks

## Logic Synthesis and Verification Using Testing Techniques

Foreword by Randal E. Bryant

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# Reasoning In Boolean Networks Logic Synthesis And Verification Using Testing Techniques

Alfredo Benso,Paolo Prinetto

**Reasoning In Boolean Networks Logic Synthesis And Verification Using Testing Techniques:**

Reasoning in Boolean Networks Wolfgang Kunz,Dominik Stoffel,2013-03-09 Reasoning in Boolean Networks provides a detailed treatment of recent research advances in algorithmic techniques for logic synthesis test generation and formal verification of digital circuits The book presents the central idea of approaching design automation problems for logic level circuits by specific Boolean reasoning techniques While Boolean reasoning techniques have been a central element of two level circuit theory for many decades Reasoning in Boolean Networks describes a basic reasoning methodology for multi level circuits This leads to a unified view on two level and multi level logic synthesis The presented reasoning techniques are applied to various CAD problems to demonstrate their usefulness for today s industrially relevant problems Reasoning in Boolean Networks provides lucid descriptions of basic algorithmic concepts in automatic test pattern generation logic synthesis and verification and elaborates their intimate relationship to provide further intuition and insight into the subject Numerous examples are provide for ease in understanding the material Reasoning in Boolean Networks is intended for researchers in logic synthesis VLSI testing and formal verification as well as for integrated circuit designers who want to enhance their understanding of basic CAD methodologies **Logic Synthesis and Verification** Soha Hassoun,Tsutomu Sasao,2012-12-06 Research and development of logic synthesis and verification have matured considerably over the past two decades Many commercial products are available and they have been critical in harnessing advances in fabrication technology to produce today s plethora of electronic components While this maturity is assuring the advances in fabrication continue to seemingly present unwieldy challenges Logic Synthesis and Verification provides a state of the art view of logic synthesis and verification It consists of fifteen chapters each focusing on a distinct aspect Each chapter presents key developments outlines future challenges and lists essential references Two unique features of this book are technical strength and comprehensiveness The book chapters are written by twenty eight recognized leaders in the field and reviewed by equally qualified experts The topics collectively span the field Logic Synthesis and Verification fills a current gap in the existing CAD literature Each chapter contains essential information to study a topic at a great depth and to understand further developments in the field The book is intended for seniors graduate students researchers and developers of related Computer Aided Design CAD tools From the foreword The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book Their innovative work contributed to design automation tools that permanently changed the course of electronic design by Aart J de Geus Chairman and CEO Synopsys Inc **Verification by Error Modeling** Katarzyna Radecka,Zeljko Zilic,2005-12-17 1 DESIGN FLOW Integrated circuit IC complexity is steadily increasing ICs incorporating hundreds of millions of transistors mega bit memories complicated pipelined structures etc are now in high demand For example Intel Itanium II processor contains more than 200 million transistors including a 3 MB third level cache A billion transistor IC was said to be imminently doable by Intel fellow J Crawford at Microprocessor Forum in

October 2002 40 Obviously designing such complex circuits poses real challenges to engineers Certainly no relief comes from the competitive marketplace with increasing demands for a very narrow window of time time to market in engineering a ready product Therefore a systematic and well structured approach to designing ICs is a must Although there are no widely adhered standards for a design flow most companies have their own established practices which they follow closely for in house design processes In general however a typical product cycle includes few milestones An idea for a new product starts usually from an depth market analysis of customer needs Once a window of opportunity is found product requirements are carefully specified Ideally these parameters would not change during the design process In practice initial phases of preparing a design specification are susceptible to potential errors as it is very difficult to grasp all the details in a complex design **Advanced Formal Verification** Rolf Drechsler,2007-05-08 Advanced Formal Verification shows the latest developments in the verification domain from the perspectives of the user and the developer World leading experts describe the underlying methods of today s verification tools and describe various scenarios from industrial practice In the first part of the book the core techniques of today s formal verification tools such as SAT and BDDs are addressed In addition multipliers which are known to be difficult are studied The second part gives insight in professional tools and the underlying methodology such as property checking and assertion based verification Finally analog components have to be considered to cope with complete system on chip designs **Formal Equivalence Checking and Design Debugging** Shi-Yu Huang,Kwang-Ting (Tim) Cheng,2012-12-06 Formal Equivalence Checking and Design Debugging covers two major topics in design verification logic equivalence checking and design debugging The first part of the book reviews the design problems that require logic equivalence checking and describes the underlying technologies that are used to solve them Some novel approaches to the problems of verifying design revisions after intensive sequential transformations such as retiming are described in detail The second part of the book gives a thorough survey of previous and recent literature on design error diagnosis and design error correction This part also provides an in depth analysis of the algorithms used in two logic debugging software programs ErrorTracer and AutoFix developed by the authors From the Foreword With the adoption of the static sign off approach to verifying circuit implementations the application specific integrated circuit ASIC industry will experience the first radical methodological revolution since the adoption of logic synthesis Equivalence checking is one of the two critical elements of this methodological revolution This book is timely for either the designer seeking to better understand the mechanics of equivalence checking or for the CAD researcher who wishes to investigate well motivated research problems such as equivalence checking of retimed designs or error diagnosis in sequential circuits Kurt Keutzer University of California Berkeley Delay Fault Testing for VLSI Circuits Angela Krstic,Kwang-Ting (Tim) Cheng,2012-12-06 In the early days of digital design we were concerned with the logical correctness of circuits We knew that if we slowed down the clock signal sufficiently the circuit would function correctly With improvements in the semiconductor process technology

our expectations on speed have soared A frequently asked question in the last decade has been how fast can the clock run This puts significant demands on timing analysis and delay testing Fueled by the above events a tremendous growth has occurred in the research on delay testing Recent work includes fault models algorithms for test generation and fault simulation and methods for design and synthesis for testability The authors of this book Angela Krstic and Tim Cheng have personally contributed to this research Now they do an even greater service to the profession by collecting the work of a large number of researchers In addition to expounding such a great deal of information they have delivered it with utmost clarity To further the reader s understanding many key concepts are illustrated by simple examples The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice In that sense this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems Tech niques for path delay testing and for use of slower test equipment to test high speed circuits are of particular interest **Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation** Alfredo Benso,Paolo Prinetto,2005-12-15 Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation intends to be a comprehensive guide to Fault Injection techniques used to evaluate the dependability of a digital system The description and the critical analysis of different Fault Injection techniques and tools will be authored by key scientists in the field of system dependability and fault tolerance      Theory and Applications of Satisfiability Testing – SAT 2008 Hans Kleine Büning,Zhao Xishunb,2008-04-25 This volume contains the papers presented at the 11th International Conference on Theory and Applications of Satis ability Testing SAT 2008 The series of International Conferences on Theory and Applications of S is ability Testing SAT has evolved from a rst workshop on SAT in 1996 to an annual international conference which is a platform for researchers studying various aspects of the propositional satis ability problem and its applications In the past the SAT conference venue alternated between Europe and North America For the rst time the conference venue was in Asia more precisely at the Zhudao Guest House near Sun Yat Sen University in Guangzhou P R China Many hard combinatorial problems can be encoded into SAT Therefore provementsonheuristics onthe practicalside as wellastheoreticalinsightsinto SAT apply to a large range of real world problems More speci cally many portant practical veri cation problems can be rephrased as SAT problems This applies to veri cation problems in hardware and software Thus SAT is bec ing one of the most important core technologies to verify secure and dependable systems The topics of the conference span practical and theoretical research on SAT and its applications and include but are not limited to proof systems proof complexity search algorithms heuristics analysis of algorithms hard instances randomized formulae problem encodings industrial applications solvers s pli ers tools case studies and empirical results SAT is interpreted in a rather broad sense besides propositional satis ability it includes for example the main of quanti ed Boolean formulae QBF and satis ability modulo theories SMT      **A Designer's Guide to Built-In Self-Test** Charles E. Stroud,2005-12-27 A recent technological advance is the art of

designing circuits to test themselves referred to as a Built In Self Test This book is written from a designer s perspective and describes the major BIST approaches that have been proposed and implemented along with their advantages and limitations

**On-Line Testing for VLSI** Michael Nicolaidis,Yervant Zorian,Dhiraj Pradhan,2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers        **Research Perspectives and Case Studies in System Test and Diagnosis** John W. Sheppard,William R. Simpson,2012-12-06 System level testing is becoming increasingly important It is driven by the incessant march of complexity which is forcing us to renew our thinking on the processes and procedures that we apply to test and diagnosis of systems In fact the complexity defines the system itself which for our purposes is any aggregation of related elements that together form an entity of sufficient complexity for which it is impractical to treat all of the elements at the lowest level of detail System approaches embody the partitioning of problems into smaller inter related subsystems that will be solved together Thus words like hierarchical dependence inference model and partitioning are frequent throughout this text Each of the authors deals with the complexity issue in a similar fashion but the real value in a collected work such as this is in the subtle differences that may lead to synthesized approaches that allow even more progress The works included in this volume are an outgrowth of the 2nd International Workshop on System Test and Diagnosis held in Alexandria Virginia in April 1998 The first such workshop was held in Freiburg Germany six years earlier In the current workshop nearly 50 experts from around the world struggled over issues concerning the subject In this volume a select group of workshop participants was invited to provide a chapter that expanded their workshop presentations and incorporated their workshop interactions While we have attempted to present the work as one volume and requested some revision to the work the content of the individual chapters was not edited significantly Consequently you will see different approaches to solving the same problems and occasional disagreement between authors as to definitions or the importance of factors The works collected in this volume represent the state of the art in system test and diagnosis and the authors are at the leading edge ofthat science From the Preface        Defect Oriented Testing for CMOS Analog and Digital Circuits Manoj Sachdev,2013-06-29 Defect oriented testing is expected to play a significant role in coming generations of

technology Smaller feature sizes and larger die sizes will make ICs more sensitive to defects that can not be modeled by traditional fault modeling approaches Furthermore with increased level of integration an IC may contain diverse building blocks Such blocks include digital logic PLAs volatile and non volatile memories and analog interfaces For such diverse building blocks traditional fault modeling and test approaches will become increasingly inadequate Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits ICs have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives Defect Oriented Testing for CMOS Analog and Digital Circuits is the first book to provide a complete overview of the subject It is essential reading for all design and test professionals as well as researchers and students working in the field A strength of this book is its breadth Types of designs considered include analog and digital circuits programmable logic arrays and memories Having a fault model does not automatically provide a test Sometimes design for testability hardware is necessary Many design for testability ideas supported by experimental evidence are included from the Foreword by Vishwani D Agrawal **High Performance Memory Testing** R. Dean Adams,2005-12-29 Are memory applications more critical than they have been in the past Yes but even more critical is the number of designs and the sheer number of bits on each design It is assured that catastrophes which were avoided in the past because memories were small will easily occur if the design and test engineers do not do their jobs very carefully High Performance Memory Testing Design Principles Fault Modeling and Self Test is based on the author s 20 years of experience in memory design memory reliability development and memory self test High Performance Memory Testing Design Principles Fault Modeling and Self Test is written for the professional and the researcher to help them understand the memories that are being tested **Power-Constrained Testing of VLSI Circuits** Nicola Nicolici,Bashir M. Al-Hashimi,2006-04-11 This text focuses on techniques for minimizing power dissipation during test application at logic and register transfer levels of abstraction of the VLSI design flow It surveys existing techniques and presents several test automation techniques for reducing power in scan based sequential circuits and BIST data paths Elements of STIL Gregory A. Maston,Tony R. Taylor,Julie N. Villar,2012-12-06 Standard Test In terface _____ Language So I was wrong I was absolutely sure that by having an IEEE Standard defined reviewed and accepted that I wouldn t need to write a book about it as well The Standard would be the complete reference And be aware this book does not serve as a replacement to the IEEE Std 1450 document You should have a copy of the Standard as you go through this book I realized that the Standard would not be the complete reference about the time that the Working Group started to put notes into the draft proposa notes to elaborate

decisions in the Working Group but that would be removed in the final draft Then once the Standard was accepted I became the central point of contact for people who just picked up the Standard who didn t have the benefit of the Working Group discussions who only had available that one final sentence in the Standard and who didn t benefit from the perspective of where those words came from Sometimes those questions have resulted in clarifications to the Standard Sometimes I would respond to those questions with more background and perspective as well It is this additional background and perspective I hope you find in this book **SOC (System-on-a-Chip) Testing for Plug and Play Test Automation** Krishnendu Chakrabarty,2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits M. Bushnell,Vishwani Agrawal,2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device techn ogy circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signalsubsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers **Test Resource Partitioning for System-on-a-Chip** Vikram Iyengar,Anshuman Chandra,2012-12-06 Test Resource Partitioning for System on a Chip is about test resource partitioning and optimization techniques for plug and play system on a chip SOC test automation Plug and play refers to the paradigm in which core to core interfaces as well as core to SOC logic interfaces

are standardized such that cores can be easily plugged into virtual sockets on the SOC design and core tests can be plugged into the SOC during test without substantial effort on the part of the system integrator The goal of the book is to position test resource partitioning in the context of SOC test automation as well as to generate interest and motivate research on this important topic SOC integrated circuits composed of embedded cores are now commonplace Nevertheless There remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and test challenges are a major contributor to the widening gap between design capability and manufacturing capacity Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols Test Resource Partitioning for System on a Chip responds to a pressing need for a structured methodology for SOC test automation It presents new techniques for the partitioning and optimization of the three major SOC test resources test hardware testing time and test data volume Test Resource Partitioning for System on a Chip paves the way for a powerful integrated framework to automate the test flow for a large number of cores in an SOC in a plug and play fashion The framework presented allows the system integrator to reduce test cost and meet short time to market requirements

**Computer Aided Verification** Swarat Chaudhuri,Azadeh Farzan,2016-07-12 The two volume set LNCS 9779 and LNCS 9780 constitutes the refereed proceedings of the 28th International Conference on Computer Aided Verification CAV 2016 held in Toronto ON USA in July 2016 The total of 46 full and 12 short papers presented in the proceedings was carefully reviewed and selected from 195 submissions The papers were organized in topical sections named probabilistic systems synthesis constraint solving model checking program analysis timed and hybrid systems verification in practice concurrency and automata and games **Boundary-Scan Interconnect Diagnosis** José T. de Sousa,Peter Y.K. Cheung,2005-12-28 Boundary Scan Interconnect Diagnosis explains how to synthesize digital diagnostic sequences for wire interconnects using boundary scan and how to assess the quality of those sequences Its importance has to do with designing complex electronic systems using pre designed intellectual property IP cores which is becoming increasingly popular nowadays Since tests for pre designed cores can be supplied with the cores themselves the only additional tests that need to be developed to test and diagnose the entire system are those for wire interconnects between the cores Besides the trivial solutions that are often used to solve this problem there are many more methods that enable significant optimizations of test vector length and or diagnostic resolution The book surveys all existing methods of this kind and proposes new ones In the new approach circuit and interconnect faults are carefully modeled and graph techniques are applied to solve the problem The original feature of the new method is the fact that it can be adjusted to provide shorter test sequences and or greater diagnostic resolution The effectiveness of existing and proposed methods is then evaluated using real electronic assemblies and published statistical data for an actual manufacturing process from HP

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