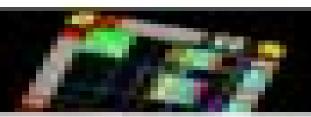
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Proceedings of the 2015 26th International Symposium on Rapid System Prototyping ,2015 the 2019 30th International Workshop on Rapid System Prototyping ,2019 The 19th IEEE/Ifip International Symposium on Rapid System Prototyping (Rsp 2008), 2008-01-01 Twenty six papers from the June 2008 symposium explore new ways to model design validate and verify software and hardware systems to meet the ever increasing demand for complex systems The contributors share their research on system specification embedded software design MPSoC and FPGA design verification and image processing Topics include an executable specification language for prototyping concurrent systems automation of communication refinement and hardware synthesis statistical codec designs in H 264 AVC standard and a flexible network intrusion detection system No subject index is provided 15th IEEE International Workshop on Rapid System Prototyping ,2004 12th International Workshop on Rapid System Prototyping ,2001 12th International Workshop on Rapid System Prototyping IEEE Computer Society. Design Automation Technical Committee, 2001 The proceedings from the June 2001 conference in Monterey California include 30 papers on hardware case studies reconfiguring computing communications systems distributed prototyping systems modeling model based prototyping efficient evaluation methodologies and tools Keynote addresses on Programming Environments for Massively Parallel Distributed Systems Karsten M. Decker, Rene M. Rehmann, 2013-04-17 Massively Parallel Systems MPSs with their scalable computation and storage space promises are becoming increasingly important for high performance computing The growing

acceptance of MPSs in academia is clearly apparent However in industrial companies their usage remains low The programming of MPSs is still the big obstacle and solving this software problem is sometimes referred to as one of the most challenging tasks of the 1990 s The 1994 working conference on Programming Environments for Massively Parallel Systems was the latest event of the working group WG 10 3 of the International Federation for Information Processing IFIP in this field It succeeded the 1992 conference in Edinburgh on Programming Environments for Parallel Computing The research and development work discussed at the conference addresses the entire spectrum of software problems including virtual machines which are less cumbersome to program more convenient programming models advanced programming languages and especially more sophisticated programming tools but also algorithms and applications **Proceedings**, 11th International Workshop on Rapid System Prototyping ,2000 Single Stage to Orbit Andrew J. Butrica, 2003-10-22 While the glories and tragedies of the space shuttle make headlines and move the nation the story of the shuttle forms an inseparabe part of a lesser known but no less important drama the search for a reusable single stage to orbit rocket Here an award winning student of space science Andrew J Butrica examines the long and tangled history of this ambitious concept from it first glimmerings in the 1920s when technicians dismissed it as unfeasible to its highly expensive heyday in the midst of the Cold War when conservative backed government programs struggled to produce an operational flight vehicle Butrica finds a blending of far sighted engineering and heavy handed politics To the first and oldest idea that of the reusable rocket powered single stage to orbit vehicle planners who belonged to what President Eisenhower referred to as the military industrial complex added experimental X aircraft like capabilties and eventually a faster cheaper smaller managerial approach Single Stage to Orbit traces the interplay of technology corporate interest and politics a combination that well served the conservative space agenda and ultimately triumphed not in the realization of inexpensive reliable space transport but in a vision of space militarization and commercialization that would appear settled United States policy in the early twenty first century D M Ashford Transactions on High-Performance Embedded Architectures and Compilers IV Per Stenström, 2011-11-15 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases. The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This 4th issue contains 21 papers carefully reviewed and selected out of numerous submissions and is divided in four sections. The first section contains five regular papers. The second section consists of the top four papers from the 4th International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2009 held in Paphos Cyprus in January 2009 The third section contains a set of six papers providing a snap shot from the

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