European Low-Power Initiative for Electronic System Design

Principles of Asynchronous Circuit Design

A Systems Perspective

Edited by
Jens Sparsø
Steve Furber

Series Editors
René van Leuken, Reinder Nouta
Alexander de Graaf

esprit

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Principles Of Asynchronous Circuit Design A Systems Perspective

Michael Seilmaier

Principles Of Asynchronous Circuit Design A Systems Perspective:

Principles of Asynchronous Circuit Design Jens Sparsø,Steve Furber,2013-04-17 Principles of Asynchronous Circuit Design A Systems Perspective addresses the need for an introductory text on asynchronous circuit design Part I is an 8 chapter tutorial which addresses the most important issues for the beginner including how to think about asynchronous systems Part II is a 4 chapter introduction to Balsa a freely available synthesis system for asynchronous circuits which will enable the reader to get hands on experience of designing high level asynchronous systems Part III offers a number of examples of state of the art asynchronous systems to illustrate what can be built using asynchronous techniques The examples range from a complete commercial smart card chip to complex microprocessors The objective in writing this book has been to enable industrial designers with a background in conventional clocked design to be able to understand asynchronous design sufficiently to assess what it has to offer and whether it might be advantageous in their next design task

Introduction to Asynchronous Circuit Design Jens Sparsø,2020-06-18 This book is an introduction to the design of asynchronous circuits It is an updated and significantly extended version of an eight chapter tutorial that first appeared as Part I in the book Principles of asynchronous circuit design A systems perspective edited by Spars and Furber 2001 a book that has become a standard reference on the topic The extensions include improved coverage of data flow components a new chapter on two phase bundled data circuits a new chapter on metastability arbitration and synchronization and a new chapter on performance analysis using timed Petri nets With these extensions the text now provides a more complete coverage of the topic and it is now made available as a stand alone book The book is a beginner s text and the amount of formal notation is deliberately kept at a minimum using instead plain English and graphical illustrations to explain the underlying intuition and reasoning behind the concepts and methods covered The book targets senior undergraduate and graduate students in Electrical and Computer Engineering and industrial designers with a background in conventional clocked digital design who wish to gain an understanding of asynchronous circuit design *Cryptographic Hardware and Embedded Systems - CHES 2006* Louis Goubin,Mitsuru Matsui,2006-10-17 This book constitutes the refereed proceedings of the 8th International Workshop on Cryptographic Hardware and Embedded Systems CHES 2006 held in Yokohama Japan in October 2006 The 32 revised full papers presented together with three invited talks were carefully reviewed and selected from 112 submissions **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** Nadine Azemard,2007-08-21 This volume features the refereed proceedings of the 17th International Workshop on Power and Timing Modeling Optimization and Simulation Papers cover high level design low power design techniques low power analog circuits statistical static timing analysis power modeling and optimization low power routing optimization security and asynchronous design low power applications modeling and optimization and more **Integrated Circuit and System Design** Enrico Macii,Vassilis Paliouras,Odysseas Koufopavlou,2004-09-07 This book constitutes the refereed

proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation PATMOS 2004 held in Santorini Greece in September 2004 The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted The papers are organized in topical sections on buses and communication circuits and devices low power issues architectures asynchronous circuits systems design interconnect and physical design security and safety low power processing digital design and modeling and simulation Advancing Embedded Systems and Real-Time Communications with Emerging Technologies Virtanen, Seppo,2014-04-30 Embedded systems and real time computing can be useful tools for a variety of applications Further research developments in this field can assist in promoting the future development of these technologies for various applications Advancing Embedded Systems and Real Time Communications with Emerging Technologies discusses embedded systems communication system engineering and real time systems in an integrated manner This research book includes advancements in the fields of computer science computer engineering and telecommunication engineering in regard to how they are used in embedded and real time systems for communications purposes With its practical and theoretical research this book is an essential reference for academicians students researchers practitioners and IT professionals **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** José L. Ayala,Delong Shang,Alex Yakovlev,2013-01-03 This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design PATMOS 2012 held in Newcastle UK Spain in September 2012 The 25 revised full papers presented were carefully reviewed and selected from numerous submissions The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems including reconfigurable hardware such as FPGAs The technical program focus on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization

Proceedings of the International Conference on Human-centric Computing 2011 and Embedded and Multimedia Computing 2011 James J. Park,Hai Jin,Xiaofei Liao,Ran Zheng,2011-07-21 Proceedings of the International Conference on Human centric Computing and Embedded and Multimedia Computing HumanCom however such devices exist simply to obtain inputs from the human and are embedded in objects that humans interact with on a daily basis Moreover during the past couple of decades Information Science technologies influenced and changed every aspect of our lives and our cultures Without various Information Science technology based applications it would be difficult to keep information stored securely to process information efficiently and to communicate conveniently Embedded computing ranges from portable devices such as digital watches and MP3 players to large stationary installations like traffic lights factory controllers or the systems controlling nuclear power plants Complexity varies from low with a single microcontroller chip to very high with multiple units peripherals and networks mounted inside a large chassis or enclosure Multimedia computing covers multimedia I O

devices OS storage systems streaming media middleware continuous media representations media coding media processing etc and also includes multimedia communications real time protocols end to end streaming media resource allocation multicast protocols and multimedia applications databases distributed collaboration video conferencing 3D virtual environments Interconnect-Centric Design for Advanced SOC and NOC Jari Nurmi,H. Tenhunen,J. Isoaho,Axel Jantsch,2006-03-20 In Interconnect centric Design for Advanced SoC and NoC we have tried to create a comprehensive understanding about on chip interconnect characteristics design methodologies layered views on different abstraction levels and finally about applying the interconnect centric design in system on chip design Traditionally on chip communication design has been done using rather ad hoc and informal approaches that fail to meet some of the challenges posed by next generation SOC designs such as performance and throughput power and energy reliability predictability synchronization and management of concurrency To address these challenges it is critical to take a global view of the communication problem and decompose it along lines that make it more tractable We believe that a layered approach similar to that defined by the communication networks community should also be used for on chip communication design The design issues are handled on physical and circuit layer logic and architecture layer and from system design methodology and tools point of view Formal communication modeling and refinement is used to bridge the communication layers and network centric modeling of multiprocessor on chip networks and socket based design will serve the development of platforms for SoC and NoC integration Interconnect centric Design for Advanced SoC and NoC is concluded by two application examples interconnect and memory organization in SoCs for advanced set top boxes and TV and a case study in NoC platform design for more generic applications **Synchronization and Arbitration in Digital Systems** David J. Kinniment,2008-02-28 Today s networks of processors on and off chip operating with independent clocks need effective synchronization of the data passing between them for reliability When two or more processors request access to a common resource such as a memory an arbiter has to decide which request to deal with first Current developments in integrated circuit processing are leading to an increase in the numbers of independent digital processing elements in a single system With this comes faster communications more networks on chip and the demand for more reliable more complex and higher performance synchronizers and arbiters Written by one of the foremost researchers in this area of digital design this authoritative text provides in depth theory and practical design solutions for the reliable working of synchronization and arbitration hardware in digital systems The book provides methods for making real reliability measurements both on and off chip evaluating some of the common difficulties and detailing circuit solutions at both circuit and system levels Synchronization and Arbitration in Digital Systems also presents mathematical models used to estimate mean time between failures in digital systems a summary of serial and parallel communication techniques for on chip data transmission explanations on how to design a wrapper for a locally synchronous cell highlighting the issues associated with stoppable clocks an examination of various

types of priority arbiters using signal transition graphs to show the specification of different designs from the simplest to more complex multi way arbiters including ways of solving problems encountered in a wide range of applications essential information on systems composed of independently timed regions including a discussion on the problem of choice and the factors affecting the time taken to make choices in electronics With its logical approach to design methodology this will prove an invaluable guide for electronic and computer engineers and researchers working on the design of digital electronic hardware Postgraduates and senior undergraduate students studying digital systems design as part of their electronic engineering course will struggle to find a resource that better details the information given inside this book Emerging Topics in Hardware Security Mark Tehranipoor,2021-04-30 This book provides an overview of emerging topics in the field of hardware security such as artificial intelligence and quantum computing and highlights how these technologies can be leveraged to secure hardware and assure electronics supply chains The authors are experts in emerging technologies traditional hardware design and hardware security and trust Readers will gain a comprehensive understanding of hardware security problems and how to overcome them through an efficient combination of conventional approaches and emerging technologies enabling them to design secure reliable and trustworthy hardware **A Designer's Guide to Asynchronous VLSI** Peter A. Beerel,Recep O. Ozdag,Marcos Ferretti,2010-02-04 Create low power higher performance circuits with shorter design times using this practical guide to asynchronous design This practical alternative to conventional synchronous design enables performance close to full custom designs with design times that approach commercially available ASIC standard cell flows It includes design trade offs specific design examples and end of chapter exercises Emphasis throughout is placed on practical techniques and real world applications making this ideal for circuit design students interested in alternative design styles and system on chip circuits as well as circuit designers in industry who need new solutions to old problems

Hardware and Software: Verification and Testing Ofer Strichman,Rachel Tzoref-Brill,2017-11-11 This book constitutes the refereed proceedings of the 13th International Haifa Verification Conference HVC 2017 held in Haifa Israel in November 2017 The 13 revised full papers presented together with 4 poster and 5 tool demo papers were carefully reviewed and selected from 45 submissions They are dedicated to advance the state of the art and state of the practice in verification and testing and are discussing future directions of testing and verification for hardware software and complex hybrid systems

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Vassilis Paliouras,Johan Vounckx,Diederik Verkest,2005-08-25 Welcome to the proceedings of PATMOS 2005 the 15th in a series of international workshops PATMOS2005wasorganizedbyIMECwithtechnicalco sponsorshipfrom the IEEE Circuits and Systems Society Over the years PATMOS has evolved into an important European event where searchers from both industry and academia discuss and investigate the emerging ch lenges in future and contemporary applications design methodologies and tools quired for the developmentof upcominggenerationsof integrated circuits and systems The technical program of PATMOS 2005

contained state of the art technical contri tions three invited talks a special session on hearing aid design and an embedded torial The technical program focused on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design char terization analysis and optimization in the nanometer era The Technical Program Committee with the assistance of additional expert revi ers selected the 74 papers to be presented at PATMOS The papers were divided into 11 technical sessions and 3 poster sessions As is always the case with the PATMOS workshops the review process was anonymous full papers were required and several reviews were carried out per paper Beyond the presentations of the papers the PATMOS technical program was riched by a series of speeches offered by world class experts on important emerging research issues of industrial relevance Prof Jan Rabaey Berkeley USA gave a talk on Traveling the Wild Frontier of Ulta Low Power Design Dr Sung Bae Park S sung gave a presentation on DVL Deep Low Voltage Circuits and Devices Prof *Communicating Sequential Processes. The First 25 Years* Ali E. Abdallah,Cliff B. Jones,Jeff W. Sanders,2005-05-04 This volume like the symposium CSP25 which gave rise to it commemorates the semi jubilee of Communicating Sequential Processes 1 Tony Hoare s paper Communicating Sequential Processes is today widely regarded as one of the most in uential papers in computer science To comm orate it an event was organized under the auspices of BCS FACS the British Computer Society s Formal Aspects of Computing Science specialist group CSP25 was one of a series of such events organized to highlight the use of formal methods emphasize their relevance to modern computing and promote their wider application BCS FACS is proud that Tony Hoare presented his original ideas on CSP at one of its rst meetings in 1978 The two day event 7 8 July 2004 was hosted by London South Bank U versity s Institute for Computing Research Faculty of Business Computing and Information Management The intention was to celebrate re ect upon and look beyondthe rstquarter centuryofCSP scontributionstocomputerscience The meeting examined the impact of CSP on many areas stretching from semantics mathematical models for understanding concurrency and communications and logic forreasoningaboutbehavior throughthedesignofparallelprogramming languages i o parallelism synchronization and threads to applications va ing from distributed software and parallel computing to information security Web services and concurrent hardware circuits It included a panel discussion with panelists Brookes Hoare de Roever and Roscoe chaired by Je Sanders poster presentations by PhD students and others featured a re alarm requ ing evacuation in the rain and concluded with the presentation of a fountain pen to Prof Sir C A R Hoare **Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation** Rene van Leuken,Gilles Sicard,2011-02-04 This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble France in September 2010 The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows circuit techniques low power circuits self timed circuits process variation high level modeling of poweraware heterogeneous designs in SystemC AMS and minalogic *Asynchronous On-Chip*

Networks and Fault-Tolerant Techniques Wei Song,Guangda Zhang,2022-05-10 Asynchronous On Chip Networks and Fault Tolerant Techniques is the first comprehensive study of fault tolerance and fault caused deadlock effects in asynchronous on chip networks aiming to overcome these drawbacks and ensure greater reliability of applications As a promising alternative to the widely used synchronous on chip networks for multicore processors asynchronous on chip networks can be vulnerable to faults even if they can deliver the same performance with much lower energy and area compared with their synchronous counterparts faults can not only corrupt data transmission but also cause a unique type of deadlock By adopting a new redundant code along with a dynamic fault detection and recovery scheme the authors demonstrate that asynchronous on chip networks can be efficiently hardened to tolerate both transient and permanent faults and overcome fault caused deadlocks This book will serve as an essential guide for researchers and students studying interconnection networks fault tolerant computing asynchronous system design circuit design and on chip networking as well as for professionals interested in designing fault tolerant and high throughput asynchronous circuits *Synaptic Circuits and Functions in Bio-inspired Integrated Architectures* Ole Richter,2024-10-15 Based upon the most advanced human made technology on this planet CMOS integrated circuit technology this dissertation examines the design of hardware components and systems to establish a technological foundation for the application of future breakthroughs in the intersection of AI and neuroscience Humans have long imagined machines robots and computers that learn and display intelligence akin to animals and themselves To advance the development of these machines specialised research in custom built hardware designed for specific types of computation which mirrors the structure of powerful biological nervous systems is especially important This dissertation is driven by the quest to harness biological and artificial neural principles to enhance the efficiency adaptability and intelligence of electronic neurosynaptic and neuromorphic hardware systems It investigates the hardware design of bio inspired neural components and their integration into more extensive scale and efficient chip architectures suitable for edge processing and near sensor environments Exploring all steps to the creation of a custom chip this work selectively surveys and advances the state of the art in bio inspired mixed signal subthreshold integrated design for neurosynaptic systems in a practical fashion Further it presents a novel asynchronous digital convolutional neuronal network processing pipeline integrated with a vision sensor for smart sensing In conclusion it sets forth a series of open challenges and future directions for the field emphasizing the need for a robust future proof base for bio inspired design and the potential of asynchronous stream processor architectures *CMOS Processors and Memories* Krzysztof Iniewski,2010-08-09 CMOS Processors and Memories addresses the state of the art in integrated circuit design in the context of emerging computing systems New design opportunities in memories and processor are discussed Emerging materials that can take system performance beyond standard CMOS like carbon nanotubes graphene ferroelectrics and tunnel junctions are explored CMOS Processors and Memories is divided into two parts processors and memories In the first part we start with high performance low power

processor design followed by a chapter on multi core processing They both represent state of the art concepts in current computing industry The third chapter deals with asynchronous design that still carries lots of promise for future computing needs At the end we present a hardware design space exploration methodology for implementing and analyzing the hardware for the Bayesian inference framework This particular methodology involves analyzing the computational cost and exploring candidate hardware components proposing various custom architectures using both traditional CMOS and hybrid nanotechnology CMOL The first part concludes with hybrid CMOS Nano architectures The second memory part covers state of the art SRAM DRAM and flash memories as well as emerging device concepts Semiconductor memory is a good example of the full custom design that applies various analog and logic circuits to utilize the memory cell s device physics Critical physical effects that include tunneling hot electron injection charge trapping Flash memory are discussed in detail Emerging memories like FRAM PRAM and ReRAM that depend on magnetization electron spin alignment ferroelectric effect built in potential well quantum effects and thermal melting are also described CMOS Processors and Memories is a must for anyone serious about circuit design for future computing technologies The book is written by top notch international experts in industry and academia It can be used in graduate course curriculum **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** Johan Vounckx,Nadine Azemard,2006-09-08 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more

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