

Performance Analysis of 3D Stacked Memory Architectures in High Performance Computing

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Abstract: The increasing speed of the CPU is greater than that of the RAM. The 'Memory Wall' issue, which occurs when the processor runs out of data, could occur. The I/O infrastructure is strained as the number of cores in CMPs rises because more data is needed from the memory subsystem. Memory bandwidth becomes a bottleneck in terms of performance. By layering memories on top of logic, three-dimensional integrated circuits are proposed as a solution to this problem. The widely-used compute-in-memory benchmark framework 'NeuroSim' is utilized by us to investigate the benefits of a three-dimensional design for a Neural Network application.

Keywords: 3D Stacked Memory, Compute in Memory, Monolithic 3D Integration, Neural Networks

I. INTRODUCTION

Most computer chores are done by the processor (CPU) getting data and instructions from main memory, which is usually an external memory that uses DRAMs, and then running them in order. Processors are becoming more and more efficient at a rate of about 60% per year thanks to new methods and technologies being used. On the other hand, DRAM technology and access times have been getting better at a rate of less than 10% per year. When more data needs to be retrieved from memory, the I/O system has to work harder to make sure there is enough memory speed. This type of 2D integrated circuit has the main memory and processor on two different chips. Because the bus link between chips is so long, there are a lot of capacitive loads. This makes the process of moving data from main memory to the CPU very slow and uses a lot of power. Because logic and memory don't work together as well as they should, microprocessor makers have had to come up with complicated, energy-hungry architectures that allow for out-of-order and speculative execution. To hide the delay in main memory, computers have also been made with bigger and bigger cache hierarchies. People often call these kinds of problems "Memory Wall problems." Applications that use a lot of data, like machine learning, neural network calculations, and real-time data analytics, are directly affected by the memory wall limit.

One way to deal with this problem is to bring the main memory closer to the processor die thus reducing access latencies, by using 2.5D or 3D packaging. In a 2.5D structure, the processor and memory are placed side-by-side on a silicon interposer to achieve extremely high die-to-die

interconnect density. In a 3D stacked structure, DRAM memory is stacked on top of the logic layer, bonded with vertical interconnects.

3D stacking enables an increase in bandwidth by using these dense interconnects instead of traditional I/O pins, allows for mixing dissimilar process technologies such as high-speed CMOS with high-density DRAM leading to an increase in on-chip memory capacity, as well as reductions in power requirements by reducing the number of external I/O drivers and interconnects [1].

Some issues with building in the third dimension, in the integration of different process technologies (and materials) together can be challenging. Further, reliability issues can be induced due to stress from higher tiered layers in the stack. Additionally, power dissipation has major influence as the high-power compute layers can create thermal hotspots in the stacked memory modules, especially those near the centre which are far away from the heat sink.

II. BACKGROUND STUDY

G. H. Loh [2] examines the integration of 3D DRAM in multicore computers, with the control and peripheral access circuitry being located on a distinct CMOS technology layer specifically designated for this purpose. The test cells are fabricated using vertically stacked NMOS technology, with Through-Silicon Vias employed for interconnecting the layers. This design implements a distributed architecture for DRAM ranks, utilising multiple layers instead of a single layer. This results in a 32% reduction in memory access time for a DRAM with five layers. The authors propose the utilisation of a vector bloom filter to enhance the functionality of the L2 miss handling architecture (MHA) in order to optimise the additional capacity provided by the 3D-stacked memory system. The test findings indicate that the proposed method of memory organisation is 1.75 times more efficient than alternative 3D DRAM concepts when performing memory-intensive jobs on a quad-core CPU.

D. H. Woo et al. [3] suggest a 3D-stacked memory architecture with a vertical L2 network using a large array of high-density TSVs to improve memory bandwidth even further. Their results show at least a 1.27x speedup over traditional 3D stacked DRAM architectures.

D. Lee et al. [4] explore another approach to better utilize the total potential bandwidth increase offered by TSVs for 3D stacked DRAMs. Their proposed architecture delivers an

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