LOW-ENERGY FPGAs

Architecture and Design

by
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Low Energy Fpgas Architecture And Design

Stamatis Vassiliadis,Dimitrios Soudris

Low Energy Fpgas Architecture And Design:

Low-Energy FPGAs — Architecture and Design Varghese George,Jan M. Rabaey,2001-06-30 Low Energy FPGAs Architecture and Design is a primary resource for both researchers and practicing engineers in the field of digital circuit design The book addresses the energy consumption of Field Programmable Gate Arrays FPGAs FPGAs are becoming popular as embedded components in computing platforms The programmability of the FPGA can be used to customize implementations of functions on an application basis This leads to performance gains and enables reuse of expensive silicon Chapter 1 provides an overview of digital circuit design and FPGAs Chapter 2 looks at the implication of deep submicron technology onFPGA power dissipation Chapter 3 describes the exploration environment to guide and evaluate design decisions Chapter 4 discusses the architectural optimization process to evaluate the trade offs between the flexibility of the architecture and the effect on the performance metrics Chapter 5 reviews different circuit techniques to reduce the performance overhead of some of the dominant components Chapter 6 shows methods to configure FPGAs to minimize the programming overhead Chapter 7 addresses the physical realization of some of the critical components and the final implementation of a specific low energy FPGA Chapter 8 compares the prototype array to an equivalent commercial architecture **Low-Energy FPGAs — Architecture and Design** Varghese George,Jan M. Rabaey,2012-12-06 Low Energy FPGAs Architecture and Design is a primary resource for both researchers and practicing engineers in the field of digital circuit design The book addresses the energy consumption of Field Programmable Gate Arrays FPGAs FPGAs are becoming popular as embedded components in computing platforms The programmability of the FPGA can be used to customize implementations of functions on an application basis This leads to performance gains and enables reuse of expensive silicon Chapter 1 provides an overview of digital circuit design and FPGAs Chapter 2 looks at the implication of deep submicron technology onFPGA power dissipation Chapter 3 describes the exploration environment to guide and evaluate design decisions Chapter 4 discusses the architectural optimization process to evaluate the trade offs between the flexibility of the architecture and the effect on the performance metrics Chapter 5 reviews different circuit techniques to reduce the performance overhead of some of the dominant components Chapter 6 shows methods to configure FPGAs to minimize the programming overhead Chapter 7 addresses the physical realization of some of the critical components and the final implementation of a specific low energy FPGA Chapter 8 compares the prototype array to an equivalent commercial architecture **FPGA Design Automation** Deming Chen,Jason Cong,Peichen Pan,2006 FPGA Design Automation A Survey is an up to date comprehensive survey tutorial of FPGA design automation with an emphasis on the recent developments within the past 5 to 10 years The focus is on the theory and techniques that have been or most likely will be reduced to practice It covers all major steps in FPGA design flow routing and placement circuit clustering technology mapping and architecture specific optimization physical synthesis RT level and behavior level synthesis and power optimization FPGA

Design Automation A Survey can be used as both a guide for beginners who are embarking on research in this relatively young yet exciting area and a useful reference for established researchers in this field **Design of Interconnection Networks for Programmable Logic** Guy Lemieux,David Lewis,2013-06-29 Programmable Logic Devices PLDs have become the key implementation medium for the vast majority of digital circuits designed today While the highest volume devices are still built with full fabrication rather than field programmability the trend towards ever fewer ASICs and more FPGAs is clear This makes the field of PLD architecture ever more important as there is stronger demand for faster smaller cheaper and lower power programmable logic PLDs are 90% routing and 10% logic This book focuses on that 90% that is the programmable routing the manner in which the programmable wires are connected and the circuit design of the programmable switches themselves Anyone seeking to understand the design of an FPGA needs to become lit erate in the complexities of programmable routing architecture This book builds on the state of the art of programmable interconnect by providing new methods of investigating and measuring interconnect structures as well as new programmable switch basic circuits The early portion of this book provides an excellent survey of interconnec tion structures and circuits as they exist today Lemieux and Lewis then provide a new way to design sparse crossbars as they are used in PLDs and show that the method works with an empirical validation This is one of a few routing architecture works that employ analytical methods to deal with the routing archi tecture design The analysis permits interesting insights not typically possible with the standard empirical approach **Embedded Computer Systems: Architectures, Modeling, and Simulation** Mladen Berekovic,Nikitas Dimopoulos,Stephan Wong,2008-07-07 This book constitutes the refereed proceedings of the 8th International Workshop on Systems Architectures Modeling and Simulation SAMOS 2008 held in Samos Greece in July 2008 The 24 revised full papers presented together with a contamplative keynote and additional papers of two special workshop sessions were carefully reviewed and selected from 62 submissions The papers are organized in topical sections on architecture new frontiers SoC application specific contributions system level design for heterogeneous systems programming multicores sensors and sensor networks and systems modeling and design **Fine- and Coarse-Grain Reconfigurable Computing** Stamatis Vassiliadis,Dimitrios Soudris,2007-10-12 Fine and Coarse Grain Reconfigurable Computing gives the basic concepts and building blocks for the design of Fine or FPGA and Coarse Grain Reconfigurable Architectures Recently developed integrated architecture design and software supported design flow of FPGA and coarse grain reconfigurable architecture are also described Part I consists of two extensive surveys of FPGA and Coarse Grain Reconfigurable Architectures The FPGA technology is defined which includes architecture logic block structure interconnect and configuration methods and existing fine grain reconfigurable architectures emerged from both academia and industry Additionally the implementation techniques and CAD tools developed to facilitate the implementation of a system in reconfigurable hardware by the industry and academia are provided In addition the features the advantages and limitations

of the coarse grain reconfigurable systems the specific issues that should be addressed during the design phase as well as representative existing coarse grain reconfigurable systems are explained In Part II case studies innovative research results about reconfigurable architectures and design frameworks from three projects AMDREL MOLEN and ADRES DRESC and a new classification according to microcoded architectural criteria are described Fine and Coarse Grain Reconfigurable Computing is an essential reference for researchers and professionals and can be used as a textbook by undergraduate graduate students and professors Foreword by Yale Patt Jim Smith and Mateo Valero *Tree-based Heterogeneous FPGA Architectures* Umer Farooq,Zied Marrakchi,Habib Mehrez,2012-05-17 This book presents a new FPGA architecture known as tree based FPGA architecture due to its hierarchical nature This type of architecture has been relatively unexplored despite their better performance and predictable routing behavior as compared to mesh based FPGA architectures In this book we explore and optimize the tree based architecture and we evaluate it by comparing it to equivalent mesh based FPGA architectures *Reconfigurable Computing: Architectures, Tools and Applications* Pedro C. Diniz,2007-03-19 This book constitutes the refereed proceedings of the Third International Workshop on Applied Reconfigurable Computing ARC 2007 held in Mangaratiba Brazil in March 2007 The 27 full papers and 10 short papers presented together with a late comer contribution from ARC 2006 are organized in topical sections on architectures mapping techniques and tools arithmetic and applications Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Johan Vounckx,Nadine Azemard,2006-09-08 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** Vassilis Paliouras,Johan Vounckx,Diederik Verkest,2005-08-25 Welcome to the proceedings of PATMOS 2005 the 15th in a series of international workshops PATMOS2005wasorganizedbyIMECwithtechnicalco sponsorshipfrom the IEEE Circuits and Systems Society Over the years PATMOS has evolved into an important European event where searchers from both industry and academia discuss and investigate the emerging ch lenges in future and contemporary applications design methodologies and tools quired for the developmentof upcominggenerationsof integrated circuits and systems The technical program of PATMOS 2005 contained state of the art technical contri tions three invited talks a special session on hearing aid design and an embedded torial The technical program focused on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design char terization analysis and optimization in the nanometer era The Technical Program Committee with the assistance of additional expert revi ers selected the 74 papers to be presented at PATMOS The papers

were divided into 11 technical sessions and 3 poster sessions As is always the case with the PATMOS workshops the review process was anonymous full papers were required and several reviews were carried out per paper Beyond the presentations of the papers the PATMOS technical program was riched by a series of speeches offered by world class experts on important emerging research issues of industrial relevance Prof Jan Rabaey Berkeley USA gave a talk on Traveling the Wild Frontier of Ulta Low Power Design Dr Sung Bae Park S sung gave a presentation on DVL Deep Low Voltage Circuits and Devices Prof

Handbook of Nature-Inspired and Innovative Computing Albert Y. Zomaya,2006-01-10 As computing devices proliferate demand increases for an understanding of emerging computing paradigms and models based on natural phenomena Neural networks evolution based models quantum computing and DNA based computing and simulations are all a necessary part of modern computing analysis and systems development Vast literature exists on these new paradigms and their implications for a wide array of applications This comprehensive handbook the first of its kind to address the connection between nature inspired and traditional computational paradigms is a repository of case studies dealing with different problems in computing and solutions to these problems based on nature inspired paradigms The Handbook of Nature Inspired and Innovative Computing Integrating Classical Models with Emerging Technologies is an essential compilation of models methods and algorithms for researchers professionals and advanced level students working in all areas of computer science IT biocomputing and network engineering   **Reconfigurable Computing: Architectures, Tools and Applications** Jürgen Becker,Roger Woods,Peter Athanas,Fearghal Morgan,2009-03-09 This book constitutes the refereed proceedings of the 5th International Workshop on Applied Reconfigurable Computing ARC 2009 held in Karlsruhe Germany in March 2009 The 21 full papers and 21 short papers presented together with the abstracts of 3 keynote lectures were carefully reviewed and selected from about 100 submissions The papers are organized in topical sections on FPGA security and bitstream analysis fault tolerant systems architectures place and route techniques cryptography and resource allocation and scheduling as well as on applications   **FPGA ...** ,2007   **Image Processing** Yung-Sheng Chen,2009-12-01 There are six sections in this book The first section presents basic image processing techniques such as image acquisition storage retrieval transformation filtering and parallel computing Then some applications such as road sign recognition air quality monitoring remote sensed image analysis and diagnosis of industrial parts are considered Subsequently the application of image processing for the special eye examination and a newly three dimensional digital camera are introduced On the other hand the section of medical imaging will show the applications of nuclear imaging ultrasound imaging and biology The section of neural fuzzy presents the topics of image recognition self learning image restoration as well as evolutionary The final section will show how to implement the hardware design based on the SoC or FPGA to accelerate image processing

Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO Shunpei Yamazaki,Masahiro Fujita,2016-12-27 This book describes the application of c axis aligned crystalline In Ga Zn oxide CAAC IGZO technology in

large scale integration LSI circuits The applications include Non volatile Oxide Semiconductor Random Access Memory NOSRAM Dynamic Oxide Semiconductor Random Access Memory DOSRAM central processing unit CPU field programmable gate array FPGA image sensors and etc The book also covers the device physics e g off state characteristics of the CAAC IGZO field effect transistors FETs and process technology for a hybrid structure of CAAC IGZO and Si FETs It explains an extremely low off state current technology utilized in the LSI circuits demonstrating reduced power consumption in LSI prototypes fabricated by the hybrid process A further two books in the series will describe the fundamentals and the specific application of CAAC IGZO to LCD and OLED displays Key features Outlines the physics and characteristics of CAAC IGZO FETs that contribute to favorable operations of LSI devices Explains the application of CAAC IGZO to LSI devices highlighting attributes including low off state current low power consumption and excellent charge retention Describes the NOSRAM DOSRAM CPU FPGA image sensors and etc referring to prototype chips fabricated by a hybrid process of CAAC IGZO and Si FETs *Low Power Designs in Nanodevices and Circuits for Emerging Applications* Shilpi Birla,Shashi Kant Dargar,Neha Singh,P. Sivakumar,2023-11-14 This reference textbook discusses low power designs for emerging applications This book focuses on the research challenges associated with theory design and applications towards emerging Microelectronics and VLSI device design and developments about low power consumptions The advancements in large scale integration technologies are principally responsible for the growth of the electronics industry This book is focused on senior undergraduates graduate students and professionals in the field of electrical and electronics engineering nanotechnology This book Discusses various low power techniques and applications for designing efficient circuits Covers advance nanodevices such as FinFETs TFETs CNTFETs Covers various emerging areas like Quantum Dot Cellular Automata Circuits and FPGAs and sensors Discusses applications like memory design for low power applications using nanodevices The number of options for ICs in control applications telecommunications high performance computing and consumer electronics continues to grow with the emergence of VLSI designs Nanodevices have revolutionized the electronics market and human life it has impacted individual life to make it more convenient They are ruling every sector such as electronics energy biomedicine food environment and communication This book discusses various emerging low power applications using CMOS and other emerging nanodevices **Applied Reconfigurable Computing** Kentaro Sano,Dimitrios Soudris,Michael Hübner,Pedro C. Diniz,2015-03-30 This book constitutes the refereed proceedings of the 11th International Symposium on Applied Reconfigurable Computing ARC 2015 held in Bochum Germany in April 2015 The 23 full papers and 20 short papers presented in this volume were carefully reviewed and selected from 85 submissions They are organized in topical headings named architecture and modeling tools and compilers systems and applications network on a chip cryptography applications extended abstracts of posters In addition the book contains invited papers on funded R D running and completed projects and Horizon 2020 funded projects **Field-Programmable Logic and Applications: Reconfigurable Computing Is Going**

Mainstream Manfred Glesner,Peter Zipf,Michel Renovell,2003-08-02 This book constitutes the refereed proceedings of the 12th International Conference on Field Programmable Logic and Applications FPL 2002 held in Montpellier France in September 2002 The 104 revised regular papers and 27 poster papers presented together with three invited contributions were carefully reviewed and selected from 214 submissions The papers are organized in topical sections on rapid prototyping FPGA synthesis custom computing engines DSP applications reconfigurable fabrics dynamic reconfiguration routing and placement power estimation synthesis issues communication applications new technologies reconfigurable architectures multimedia applications FPGA based arithmetic reconfigurable processors testing and fault tolerance crypto applications multitasking compilation techniques etc   Field George Dekoulis,2017-05-31 This edited volume Field Programmable Gate Array is a collection of reviewed and relevant research chapters offering a comprehensive overview of recent developments in the field of semiconductors The book comprises single chapters authored by various researchers and edited by an expert active in the aerospace engineering systems research area All chapters are complete within themselves but united under a common research study topic This publication aims at providing a thorough overview of the latest research efforts by international authors and open new possible research paths for further novel developments   *Field Programmable Logic and Applications* Peter Y.K. Cheung,Georg A. Constantinides,Jose T. de Sousa,2003-10-02 This book contains the papers presented at the 13th International Workshop on Field Programmable Logic and Applications FPL held on September 1 3 2003 The conference was hosted by the Institute for Systems and Computer Engineering Research and Development of Lisbon INESC ID and the Depa ment of Electrical and Computer Engineering of the IST Technical University of Lisbon Portugal The FPL series of conferences was founded in 1991 at Oxford University UK and has been held annually since in Oxford 3 times Vienna Prague Darmstadt London Tallinn Glasgow Villach BelfastandMontpellier Itbrings together academic researchers industrial experts users and newcomers in an formal welcomingatmospherethatencouragesproductiveexchangeofideasand knowledge between delegates Exciting advances in eld programmable logic show no sign of slowing down New grounds have been broken in architectures design techniques run time con guration and applications of eld programmable devices in several di erent areas Many of these innovations are reported in this volume The size of FPL conferences has grown signi cantly over the years FPL in 2002 saw 214 papers submitted representing an increase of 83% when compared to the year before The interest and support for FPL in the programmable logic community continued this year with 216 papers submitted The technical p gram was assembled from 90 selected regular papers and 56 posters resulting in this volume of proceedings The program also included three invited plenary keynote presentations from LSI Logic Xilinx and Cadence and three industrial tutorials from Altera Mentor Graphics and Dafca

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Table of Contents Low Energy Fpgas Architecture And Design

1. Understanding the eBook Low Energy Fpgas Architecture And Design
    - The Rise of Digital Reading Low Energy Fpgas Architecture And Design
    - Advantages of eBooks Over Traditional Books
2. Identifying Low Energy Fpgas Architecture And Design
    - Exploring Different Genres
    - Considering Fiction vs. Non-Fiction
    - Determining Your Reading Goals
3. Choosing the Right eBook Platform
    - Popular eBook Platforms
    - Features to Look for in an Low Energy Fpgas Architecture And Design
    - User-Friendly Interface
4. Exploring eBook Recommendations from Low Energy Fpgas Architecture And Design

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