

Scalable Shared-Memory Multiprocessing

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Scalable Shared-Memory Multiprocessing
by Daniel E. Joshi and
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343 pp.
\$54.95
Morgan Kaufmann
San Francisco
1994
ISBN 1-55860-315-8

This book is primarily devoted to Dash (J/Kinexory Architecture for Shared Memory), a multiprocessor system known from earlier publications (see "The Stanford Dash Multiprocessor," *Computer, Mar. 1992*, Vol. 35, No. 3, pp. 63-79). The book also provides readers with a comprehensive view of modern multiprocessing, as it describes where the technology is actually heading.

The major issue in multiprocessor architecture is communication: how multiple processors communicate with each other. Not so long ago, buses were the major component tying various computational pieces together. Multiple processors used a bus to access common memory or to communicate with separate memories, which caused a communication bottleneck. Strictly speaking, the problem started when users wanted to extend existing systems with several processors to much larger aggregates of dozens or even hundreds of processing units. In such cases, even hierarchically organized buses began to saturate, and designers faced a scalability barrier. Moving from a bus to a point-to-point network was an immediate solution, but then old problems persisted and new ones arose, such as cache coherence. One approach was to maintain shared memory (common address space) along the bus or across the network, without cache coherence. Another relied on message passing, but in both cases the memory latency problem emerged. Technological developments soon made possible widespread use of caches, and then other problems surfaced. Maintaining cache coherence across the bus (let alone the entire network) is not trivial, and most designers lost their hair before coming up with satisfactory solutions.

This book is a concentrated effort to address such problems and provide a solution to maintain cache coherence across the point-to-point network of multiple processors. The authors call it scalable shared-memory multiprocessing (SSMP). The book's three parts are General Concepts, Experience with Dash, and Future Trends. The first is the most interesting. It is mainly a historical perspective on multiprocessor systems.

The book first discusses scalability problems in detail, concluding that hardware cache coherence is a key to high performance. To ensure scalability, one must apply point-to-point interconnections (as opposed to a bus) and base cache coherence on directory schemes. Scalability has three dimensions:

- How does the performance scale? That is, when speeding (in terms of execution time) can we achieve by using N processors over a single processor for the same problem?
- How does the cost scale when more processors are added?
- What is the largest number of processors for which multiprocessing rather than uniprocessing is still advantageous? That is, what is the range of scalability?

The book then proceeds to simulation experiments for six realistic practical problems: simulation of hypersonic flow using a particle-in-cell method, water molecule interaction, digital logic simulation, routing wires for VLSI standard-cell designs, Cholesky factorization of a sparse matrix, and hierarchical N -body gravitation simulation. To study the execution behavior of all six applications, the authors ran them on a simulated multiprocessor, with shared data uncached and cached under a simple PRAM memory model. The major finding was that reducing memory latency due to shared data is crucial for achieving good performance of parallel applications. The study of communication behavior revealed that, quite obviously, real memory system models increased traffic by an order of magnitude. Finally, directory-based cache coherence using an invalidating protocol matched the applications' behavior well. The text extensively documents all six studies.

Next, the authors tackle techniques to address problems of long latency and limited bandwidth. The latency problem increases with the number of processors, because the majority of memory must be accessed through the interconnection network. Similarly, because of high cost, the bandwidth to access memory cannot increase linearly with additional processors and memory. The book discusses two approaches to handling memory latency: latency reduction and latency hiding. The authors also describe the most likely cause of bandwidth problems hot spots caused by references to synchronization variables.

The first part concludes with a discussion of implementation issues, including costs, and a critical overview of SSMP systems designed and built so far. These systems are grouped into six categories: directory-based, hierarchical, reflective memory, non-cache-coherent, server, and virtual shared-memory systems.

The authors then thoroughly describe their experience in building the Dash system, its

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Table of Contents Scalable Sharedmemory Multiprocessing

1. Understanding the eBook Scalable Sharedmemory Multiprocessing
 - The Rise of Digital Reading Scalable Sharedmemory Multiprocessing
 - Advantages of eBooks Over Traditional Books
2. Identifying Scalable Sharedmemory Multiprocessing
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Scalable Sharedmemory Multiprocessing
 - User-Friendly Interface
4. Exploring eBook Recommendations from Scalable Sharedmemory Multiprocessing
 - Personalized Recommendations
 - Scalable Sharedmemory Multiprocessing User Reviews and Ratings
 - Scalable Sharedmemory Multiprocessing and Bestseller Lists
5. Accessing Scalable Sharedmemory Multiprocessing Free and Paid eBooks
 - Scalable Sharedmemory Multiprocessing Public Domain eBooks
 - Scalable Sharedmemory Multiprocessing eBook Subscription Services
 - Scalable Sharedmemory Multiprocessing Budget-Friendly Options
6. Navigating Scalable Sharedmemory Multiprocessing eBook Formats

- ePub, PDF, MOBI, and More
- Scalable Sharedmemory Multiprocessing Compatibility with Devices
- Scalable Sharedmemory Multiprocessing Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Scalable Sharedmemory Multiprocessing
 - Highlighting and Note-Taking Scalable Sharedmemory Multiprocessing
 - Interactive Elements Scalable Sharedmemory Multiprocessing
- 8. Staying Engaged with Scalable Sharedmemory Multiprocessing
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Scalable Sharedmemory Multiprocessing
- 9. Balancing eBooks and Physical Books Scalable Sharedmemory Multiprocessing
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Scalable Sharedmemory Multiprocessing
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Scalable Sharedmemory Multiprocessing
 - Setting Reading Goals Scalable Sharedmemory Multiprocessing
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Scalable Sharedmemory Multiprocessing
 - Fact-Checking eBook Content of Scalable Sharedmemory Multiprocessing
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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