Reduced Instruction Set Computer Architecture

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Since the earliest days of the computer era, the general trend in computer architecture and organization has been toward increasing CPU complexity: large instruction sets, more addressing modes, more specialized registers, and the like. However, in the past several years, there has been increasing interest in an innovative approach to computer architecture: the reduced instruction set computer (RISC). The intended performance benefits of RISC compared to a more conventional approach, include more effective compilers, no use of microcode, more effective pipelining, and improved response to interrupts. Key characteristics of the RISC approach include: a limited and simple instruction set; the use of either a large number of registers (hundreds) or an optimizing compiler; to maximize the use of registers and minimize references to main memory; an emphasis on optimizing the instruction execution pipeline.
This paper presents a tutorial on the RISC approach and highlights the key design issues involved in RISC architecture. We begin by looking at the results of a number of studies on the instruction execution characteristics of compiled high-level language programs. The results of these studies inspired the RISC movement. The paper then summarizes approaches to these key RISC design issues: optimized register usage, reduced instruction sets, and pipelining. As examples, an experimental system, the Berkeley RISC, and a commercial system, the MIPS R2000, are presented. The paper closes with a discussion of the RISC versus CISC (complex instruction set computer) controversy.

I. INTRODUCTION

Since the development of the stored-program computer around 1950, there have been remarkably few true innovations in the areas of computer organization and architecture. One of the most interesting and, potentially, one of the most important innovations is the reduced instruction set computer (RISC). The RISC architecture is a dramatic departure from the historical trend in CPU architecture and challenges the conventional wisdom expressed in words and deeds by most computer architects. An analysis of the RISC architecture brings into focus many of the important issues in computer organization and architecture.

Most of the work has been on experimental systems. But commercial RISC systems have begun to appear [1]–[12].

Recently, both IBM (with its RT PC) and Hewlett-Packard (with its 900 series) have introduced machines that have both RISC and conventional characteristics [13], [14]. Although RISC systems have been defined and designed in a variety of ways by different groups, the key elements shared by most (not all) designs are these:

- a limited and simple instruction set;
- the use of either a hardware or compiler strategy to maximize the use of registers and minimize references to main memory;
- an emphasis on optimizing the instruction execution pipeline.

This paper surveys key design issues relating to RISC architecture. To begin, we present a brief survey of some results on instruction sets that inspired much of the RISC work.

II. INSTRUCTION EXECUTION CHARACTERISTICS

One of the most visible forms of evolution associated with computers is that of programming languages. As the cost of hardware has dropped, the relative cost of software has risen. Along with that, a chronic shortage of programmers has driven up software costs in absolute terms. Thus the major cost in the life cycle of a system is software, not hardware. Adding to the cost, and to the inconvenience, is the element of unreliability: it is common for programs, both system and application, to continue to exhibit new bugs after years of operation.

The response from researchers and industry has been to develop ever more powerful and complex high-level programming languages (compare Fortran to Ada). These high-level languages (HLL) allow the programmer to express algorithms more concisely, take care of much of the detail, and often support naturally the use of structured programming.

Alas, this solution gave rise to another problem, known as the semantic gap, the difference between the operations provided in HLLs and those provided in computer architecture. Symptoms of this gap are alleged to include execution inefficiency, excessive program size, and compiler complexity. Designers responded with architectures intended to close this gap. Key features include large

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