Self-Checking and Fault-Tolerant Digital Design

Parag K. Lala

Self Checking And Fault Tolerant Digital Design

Sudeep Pasricha,Nikil Dutt

Self Checking And Fault Tolerant Digital Design:

Self-Checking and Fault-Tolerant Digital Design Parag K. Lala,2001 With VLSI chip transistors getting smaller and smaller today s digital systems are more complex than ever before This increased complexity leads to more cross talk noise and other sources of transient errors during normal operation Traditional off line testing strategies cannot guarantee detection of these transient faults And with critical applications relying on faster more powerful chips fault tolerant self checking mechanisms must be built in to assure reliable operation Self Checking and Fault Tolerant Digital Design deals extensively with self checking design techniques and is the only book that emphasizes major techniques for hardware fault tolerance Graduate students in VLSI design courses as well as practicing designers will appreciate this balanced treatment of the concepts and theory underlying fault tolerance along with the practical techniques used to create fault tolerant systems Features Introduces reliability theory and the importance of maintainability Presents coding and the construction of several error detecting and correcting codes Discusses in depth the available techniques for fail safe design of combinational circuits Details checker design techniques for detecting erroneous bits and encoding output of self checking circuits Demonstrates how to design self checking sequential circuits including a technique for fail safe state machine design *Fault-Tolerant Systems* Israel Koren,C. Mani Krishna,2020-09-01 Fault Tolerant Systems Second Edition is the first book on fault tolerance design utilizing a systems approach to both hardware and software No other text takes this approach or offers the comprehensive and up to date treatment that Koren and Krishna provide The book comprehensively covers the design of fault tolerant hardware and software use of fault tolerance techniques to improve manufacturing yields and design and analysis of networks Incorporating case studies that highlight more than ten different computer systems with fault tolerance techniques implemented in their design the book includes critical material on methods to protect against threats to encryption subsystems used for security purposes The text s updated content will help students and practitioners in electrical and computer engineering and computer science learn how to design reliable computing systems and how to analyze fault tolerant computing systems Delivers the first book on fault tolerance design with a systems approach Offers comprehensive coverage of both hardware and software fault tolerance as well as information and time redundancy Features fully updated content plus new chapters on failure mechanisms and fault tolerance in cyber physical systems Provides a complete ancillary package including an on line solutions manual for instructors and PowerPoint slides *Code Design for Dependable Systems* Eiji Fujiwara,2006-07-21 Theoretical and practical tools to master matrix code design strategy and technique Error correcting and detecting codes are essential to improving system reliability and have popularly been applied to computer systems and communication systems Coding theory has been studied mainly using the code generator polynomials hence the codes are sometimes called polynomial codes On the other hand the codes designed by parity check matrices are referred to in this book as matrix codes This timely book focuses on the design theory for matrix codes and their practical applications

for the improvement of system reliability As the author effectively demonstrates matrix codes are far more flexible than polynomial codes as they are capable of expressing various types of code functions In contrast to other coding theory publications this one does not burden its readers with unnecessary polynomial algebra but rather focuses on the essentials needed to understand and take full advantage of matrix code constructions and designs Readers are presented with a full array of theoretical and practical tools to master the fine points of matrix code design strategy and technique Code designs are presented in relation to practical applications such as high speed semiconductor memories mass memories of disks and tapes logic circuits and systems data entry systems and distributed storage systems New classes of matrix codes such as error locating codes spotty byte error control codes and unequal error control codes are introduced along with their applications A new parallel decoding algorithm of the burst error control codes is demonstrated In addition to the treatment of matrix codes the author provides readers with a general overview of the latest developments and advances in the field of code design Examples figures and exercises are fully provided in each chapter to illustrate concepts and engage the reader in designing actual code and solving real problems The matrix codes presented with practical parameter settings will be very useful for practicing engineers and researchers References lead to additional material so readers can explore advanced topics in depth Engineers researchers and designers involved in dependable system design and code design research will find the unique focus and perspective of this practical guide and reference helpful in finding solutions to many key industry problems It also can serve as a coursebook for graduate and advanced undergraduate students   *New Methods of Concurrent Checking* Michael Gössel,Vitaly Ocheretny,Egor Sogomonyan,Daniel Marienfeld,2008-04-26 Computers are everywhere around us We for example as air passengers car drivers laptop users with Internet connection cell phone owners hospital patients inhabitants in the vicinity of a nuclear power station students in a digital library or customers in a supermarket are dependent on their correct operation Computers are incredibly fast inexpensive and equipped with almost unimag able large storage capacity Up to 100 million transistors per chip are quite common today a single transistor for each citizen of a large capital city in the world can be 2 easily accommodated on an ordinary chip The size of such a chip is less than 1 cm This is a fantastic achievement for an unbelievably low price However the very small and rapidly decreasing dimensions of the transistors and their connections over the years are also the reason for growing problems with reliability that will dramatically increase for the nano technologies in the near future Can we always trust computers Are computers always reliable Are chips suf ciently tested with respect to all possible permanent faults if we buy them at a low price or have errors due to undetected permanent faults to be discovered by c current checking Besides permanent faults many temporary or transient faults are also to be expected   **Design and Analysis of Fault-tolerant Digital Systems** Barry W. Johnson,1989   *Designing 2D and 3D Network-on-Chip Architectures* Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It

highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies

Formal Methods in Computer-Aided Design Mark D. Aagaard,John W. O'Leary,2002-10-23 This volume contains the proceedings of the Fourth Biennial Conference on F mal Methods in Computer Aided Design FMCAD The conference is devoted to the use of mathematical methods for the analysis of digital hardware c cuits and systems The workreported in this bookdescribes the use of formal mathematics and associated tools to design and verify digital hardware systems Functional veri cation has become one of the principal costs in a modern computer design e ort FMCAD provides a venue for academic and industrial researchers and practitioners to share their ideas and experiences of using screte mathematical modeling and veri cation Over the past 20 years this area has grown from just a few academic researchers to a vibrant worldwide com nity of people from both academia and industry This volume includes 23 papers selected from the 47 submitted papers each of which was reviewed by at least three program committee members The history of FMCAD dates backto 1984 when the earliest meetings on this topic occurred as part of IFIP WG10 2 **On-Line Testing for VLSI** Michael Nicolaidis,Yervant Zorian,Dhiraj Pradhan,2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers

Design and Test Technology for Dependable Systems-on-Chip Ubar, Raimund,Raik, Jaan,Vierhaus, Heinrich Theodor,2010-12-31 This book covers aspects of system design and efficient modelling and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip SoC Multi Processor System on Chip MPSoC or Network on Chip NoC *System-on-Chip Test Architectures* Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing

and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students   *An Introduction to Logic Circuit Testing* Parag K. Lala,2022-06-01 An Introduction to Logic Circuit Testing provides a detailed coverage of techniques for test generation and testable design of digital electronic circuits systems The material covered in the book should be sufficient for a course or part of a course in digital circuit testing for senior level undergraduate and first year graduate students in Electrical Engineering and Computer Science The book will also be a valuable resource for engineers working in the industry This book has four chapters Chapter 1 deals with various types of faults that may occur in very large scale integration VLSI based digital circuits Chapter 2 introduces the major concepts of all test generation techniques such as redundancy fault coverage sensitization and backtracking Chapter 3 introduces the key concepts of testability followed by some ad hoc design for testability rules that can be used to enhance testability of combinational circuits Chapter 4 deals with test generation and response evaluation techniques used in BIST built in self test schemes for VLSI chips Table of Contents Introduction Fault Detection in Logic Circuits Design for Testability Built in Self Test References   *VLSI Test Principles and Architectures* Laung-Terng Wang,Cheng-Wen Wu,Xiaoqing Wen,2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures   On-line Error Detection and Fast Recover Techniques for Dependable Embedded Processors Matthias Pflanz,2003-07-31 This book presents a new approach to on line observation and concurrent checking of processors by refining and improving known techniques and introducing new ideas The proposed on line error detection and fast recover techniques support and complement other established methods In combination with other on line observation priniciples and with a combined hardware software test these techniques are used to fulfill a complete self check scheme for an embedded processor   **Small and Medium Enterprises: Concepts, Methodologies, Tools, and Applications**

Management Association, Information Resources,2013-04-30 This book provides a comprehensive collection of research on current technological developments and organizational perspectives on the scale of small and medium enterprises Provided by publisher   *VLSI Testing* Stanley Leonard Hurst,1998 Hurst an editor at the Microelectronics Journal analyzes common problems that electronics engineers and circuit designers encounter while testing integrated circuits and the systems in which they are used and explains a variety of solutions available for overcoming them in both digital and mixed circuits Among his topics are faults in digital circuits generating a digital test pattern signatures and self tests structured design for testability testing structured digital circuits and microprocessors and financial aspects of testing The self contained reference is also suitable as a textbook in a formal course on the subject Annotation copyrighted by Book News Inc Portland OR

Integrated Circuit and System Design Enrico Macii,Vassilis Paliouras,Odysseas Koufopavlou,2004-08-24 WelcometotheproceedingsofPATMOS2004 thefourteenthinaseriesofint national workshops PATMOS 2004 was organized by the University of Patras with technical co sponsorship from the IEEE Circuits and Systems Society Over the years the PATMOS meeting has evolved into an important ropean event where industry and academia meet to discuss power and timing aspects in modern integrated circuit and system design PATMOS provides a forum for researchers to discuss and investigate the emerging challenges in sign methodologies and tools required to develop the upcoming generations of integrated circuits and systems We realized this vision this year by providing a technical program that contained state of the art technical contributions a keynote speech three invited talks and two embedded tutorials The technical program focused on timing performance and power consumption as well as architectural aspects with particular emphasis on modelling design charac rization analysis and optimization in the nanometer era This year a record 152 contributions were received to be considered for p sible presentation at PATMOS Despite the choice for an intense three day m ting only 51 lecture papers and 34 poster papers could be accommodated in the single track technical program The Technical Program Committee with the sistance of additional expert reviewers selected the 85 papers to be presented at PATMOS and organized them into 13 technical sessions As was the case with the PATMOS workshops the review process was anonymous full papers were required and several reviews were received per manuscript   **Bio-Inspired and Nanoscale Integrated Computing** Mary Mehrnoosh Eshaghian-Wilner,2009-09-22 Brings the latest advances in nanotechnology and biology to computing This pioneering book demonstrates how nanotechnology can create even faster denser computing architectures and algorithms Furthermore it draws from the latest advances in biology with a focus on bio inspired computing at the nanoscale bringing to light several new and innovative applications such as nanoscale implantable biomedical devices and neural networks Bio Inspired and Nanoscale Integrated Computing features an expert team of interdisciplinary authors who offer readers the benefit of their own breakthroughs in integrated computing as well as a thorough investigation and analyses of the literature Carefully edited the book begins with an introductory chapter providing a general overview of the field It ends with a chapter

setting forth the common themes that tie the chapters together as well as a forecast of emerging avenues of research Among the important topics addressed in the book are modeling of nano devices quantum computing quantum dot cellular automata dielectrophoretic reconfigurable nano architectures multilevel and three dimensional nanomagnetic recording spin wave architectures and algorithms fault tolerant nanocomputing molecular computing self assembly of supramolecular nanostructures DNA nanotechnology and computing nanoscale DNA sequence matching medical nanorobotics heterogeneous nanostructures for biomedical diagnostics biomimetic cortical nanocircuits bio applications of carbon nanotubes and nanoscale image processing Readers in electrical engineering computer science and computational biology will gain new insights into how bio inspired and nanoscale devices can be used to design the next generation of enhanced integrated circuits   **Reliable Computer Systems** Daniel Siewiorek,Robert Swarz,2014-06-28 Enhance your hardware software reliability Enhancement of system reliability has been a major concern of computer users and designers and this major revision of the 1982 classic meets users continuing need for practical information on this pressing topic Included are case studies of reliable systems from manufacturers such as Tandem Stratus IBM and Digital as well as coverage of special systems such as the Galileo Orbiter fault protection system and AT T telephone switching processors   Reliable Computer Systems Daniel P. Siewiorek,Robert S. Swarz,1998-12-15 This classic reference work is a comprehensive guide to the design evaluation and use of reliable computer systems It includes case studies of reliable systems from manufacturers such as Tandem Stratus IBM and Digital It covers special systems such as the Galileo Orbiter fault protection system and AT T telephone switching system processors   *On-Chip Communication Architectures* Sudeep Pasricha,Nikil Dutt,2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architecures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures

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