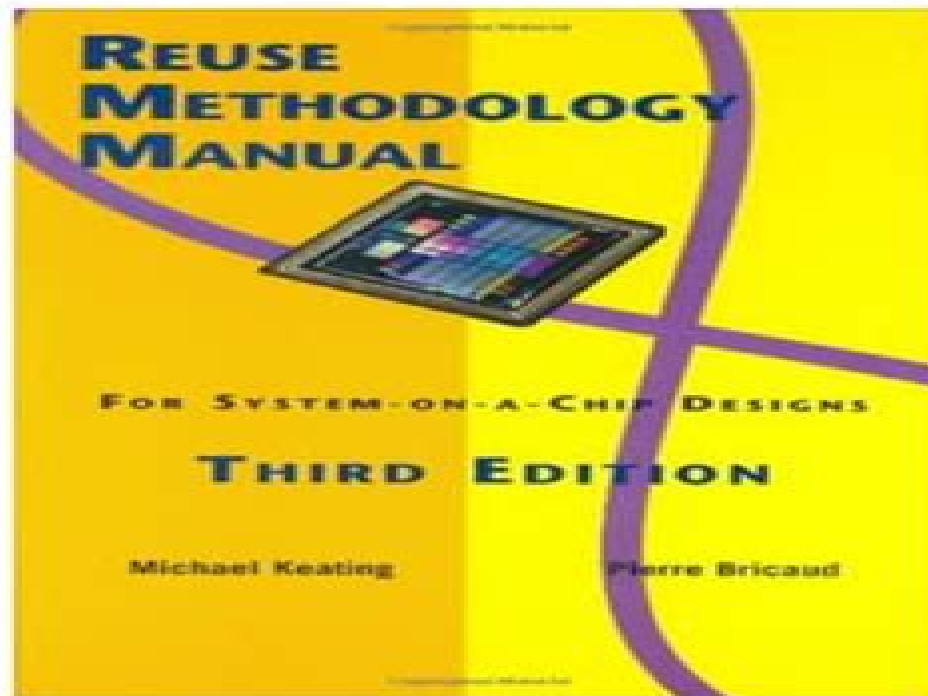


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Reuse Methodology Manual For System-on-a-Chip Designs:

Reuse Methodology Manual for System-on-a-Chip Designs Michael Keating, Pierre Bricaud, 2002 Reuse Methodology Manual for System on a Chip Designs Third Edition outlines a set of best practices for creating reusable designs for use in an SoC design methodology These practices are based on the authors experience in developing reusable designs as well as the experience of design teams in many companies around the world Silicon and tool technologies move so quickly that many of the details of design for reuse will undoubtedly continue to evolve over time But the fundamental aspects of the methodology described in this book have become widely adopted and are likely to form the foundation of chip design for some time to come Development methodology necessarily differs between system designers and processor designers as well as between DSP developers and chipset developers However there is a common set of problems facing everyone who is designing complex chips In response to these problems design teams have adopted a block based design approach that emphasizes design reuse Reusing macros sometimes called cores that have already been designed and verified helps to address all of the problems above However in adopting reuse based design design teams have run into a significant problem Reusing blocks that have not been explicitly designed for reuse has often provided little or no benefit to the team The effort to integrate a pre existing block into new designs can become prohibitively high if the block does not provide the right views the right documentation and the right functionality From this experience design teams have realized that reuse based design requires an explicit methodology for developing reusable macros that are easy to integrate into SoC designs This manual focuses on describing these techniques Features of the Third Edition Up to date State of the art Reuse as a solution for circuit designers A chronicle of best practices All chapters updated and revised Generic guidelines non tool specific Emphasis on hard IP and physical design

Reuse Methodology Manual for System-On-a-Chip Designs Pierre Bricaud, 2014-09-01

Reuse Methodology Manual for System-on-a-Chip Designs Pierre Bricaud, 2007-05-08 This revised and updated third edition outlines a set of best practices for creating reusable designs for use in an System on a Chip SoC design methodology These practices are based on the authors experience in developing reusable designs as well as the experience of design teams in many companies around the world

Reuse Methodology Manual Pierre Bricaud, 2012-12-06 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available These designers see current design tools and methodologies as inadequate for developing million gate ASICs from scratch There is considerable pressure to keep design team size and design schedules constant even as design complexities grow Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology Design reuse the use

of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs Second Edition outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process Reuse Methodology Manual for System On A Chip Designs Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high quality SoC designs *System Level Design Model with Reuse of System IP* Patrizia Cavalloro, Christophe Gendarme, Klaus Kronl f, Jean Mermet, J. van Sas, Kari Tiensyrj , Nikolaos Voros, 2007-05-08 This book addresses system design providing a framework for assessing and developing system design practices that observe and utilise reuse of system design know how The know how accumulated in the companies represents an intellectual asset or property IP System-on-a-Chip Verification Prakash Rashinkar, Peter Paterson, Leena Singh, 2007-05-08 System On a Chip Verification Methodology and Techniques is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign off The topics covered include Introduction to the SOC design and verification aspects System level verification in brief Block level verification Analog mixed signal simulation Simulation HW SW Co verification Static netlist verification Physical verification and Design sign off in brief All the verification aspects are illustrated with a single reference design for Bluetooth application System On a Chip Verification Methodology and Techniques takes a systematic approach that covers the following aspects of verification strategy in each chapter Explanation of the objective involved in performing verification after a given design step Features of options available When to use a particular option How to select an option and Limitations of the option This exciting new book will be of interest to all designers and test professionals Verification Techniques for System-Level Design Masahiro Fujita, Indradeep Ghosh, Mukul Prasad, 2010-07-27 This book will explain how to verify SoC Systems on Chip logic designs using formal and semiformal verification techniques The critical issue to be addressed is whether the functionality of the design is the one that the designers intended Simulation has been used for checking the correctness of SoC designs as in functional verification but many subtle design errors cannot be caught by simulation Recently formal verification giving mathematical proof of the correctness of designs has been gaining popularity For higher design productivity it is essential to debug designs as early as possible which this book facilitates This book covers all aspects of high level formal and semiformal verification techniques for system level designs First book that covers all aspects of formal and semiformal high level higher than RTL design verification targeting SoC designs Formal verification of high level designs RTL or higher Verification techniques are discussed with associated system level design methodology **EDA for IC System Design, Verification, and Testing**

Louis Scheffer, Luciano Lavagno, Grant Martin, 2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set *The Industrial Information Technology Handbook* Richard Zurawski, 2018-10-03 The Industrial Information Technology Handbook focuses on existing and emerging industrial applications of IT and on evolving trends that are driven by the needs of companies and by industry led consortia and organizations Emphasizing fast growing areas that have major impacts on industrial automation and enterprise integration the Handbook covers topics such as industrial communication technology sensors and embedded systems The book is organized into two parts Part 1 presents material covering new and quickly evolving aspects of IT Part 2 introduces cutting edge areas of industrial IT The Handbook presents material in the form of tutorials surveys and technology overviews combining fundamentals and advanced issues with articles grouped into sections for a cohesive and comprehensive presentation The text contains 112 contributed reports by industry experts from government companies at the forefront of development and some of the most renowned academic and research institutions worldwide Several of the reports on recent developments actual deployments and trends cover subject matter presented to the public for the first time **Embedded Systems Handbook** Richard Zurawski, 2005-08-16 Embedded systems are nearly ubiquitous and books on individual topics or components of embedded systems are equally abundant Unfortunately for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink Until now The Embedded Systems Handbook is an oasis of information offering a mix of basic a **Digital Design (Verilog)** Peter J. Ashenden, 2007-10-24 Digital Design An Embedded Systems Approach Using Verilog provides a foundation in digital design for students in computer engineering electrical engineering and computer science courses It takes an up to date and modern approach of presenting digital logic design as an activity in a larger systems design context Rather than focus on aspects of digital design that have little relevance in a realistic design context this book concentrates on modern and evolving knowledge and design skills Hardware description language HDL based design and verification is emphasized Verilog examples are used extensively throughout By treating digital logic as part of embedded systems design this book provides an understanding of the hardware needed in the analysis and design of systems comprising both hardware and software components Includes a Web site with links to vendor tools labs and tutorials Presents digital logic design as an activity in a larger systems design context Features extensive use of Verilog examples to demonstrate HDL hardware description language usage at the abstract behavioural level and register

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Electronic Design Automation for IC System Design, Verification, and Testing Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

Winning the SoC Revolution Grant Martin, Henry Chang, 2012-12-06 In 1998 99 at the dawn of the SoC Revolution we wrote *Surviving the SOC Revolution A Guide to Platform Based Design* In that book we focused on presenting guidelines and best practices to aid engineers beginning to design complex System on Chip devices SoCs Now in 2003 facing the mid point of that revolution we believe that it is time to focus on winning In this book *Winning the SoC Revolution Experiences in Real Design* we gather the best practical experiences in how to design SoCs from the most advanced design groups while setting the issues and techniques in the context of SoC design methodologies As an edited volume this book has contributions from the leading design houses who are winning in SoCs Altera ARM IBM Philips TI UC Berkeley and Xilinx These chapters present the many facets of SoC design the platform based approach how to best utilize IP Verification FPGA fabrics as an alternative to ASICs and next generation process technology issues We also include observations from Ron Wilson of CMP Media on best practices for SoC design team collaboration We hope that by utilizing this book you too will win the SoC Revolution

Formal Methods and Models for System Design Rajesh Gupta, Paul Le Guernic, Sandeep Kumar Shukla, Jean-Pierre Talpin, 2004-06-30 Perhaps nothing characterizes the inherent heterogeneity in embedded systems than the ability to choose between hardware and software implementations of a given system function Indeed most embedded

systems at their core represent a careful division and design of hardware and software parts of the system. To do this task effectively, models and methods are necessary to capture application behavior, needs, and system implementation constraints. Formal modeling can be valuable in addressing these tasks. As with most engineering domains, co-design practice defines the state of the art; it seeks to add new capabilities in system conceptualization, model transformation, optimization, and implementation. These advances, particularly those related to synthesis and verification tasks, directly depend upon formal understanding of system behavior and performance measures. Current practice in system modeling relies upon exploiting high-level programming frameworks such as SystemC, Esterel, or others to capture design at increasingly higher levels of abstraction and attempts to reduce the system implementation task. While raising the abstraction levels for design and verification tasks to be really useful, these approaches must also provide for reuse/adaptation of the existing intellectual property (IP) blocks.

Embedded Systems Handbook 2-Volume Set Richard Zurawski, 2018-10-08 During the past few years, there has been an dramatic upsurge in research and development, implementations of new technologies, and deployments of actual solutions and technologies in the diverse application areas of embedded systems. These areas include automotive electronics, industrial automated systems, and building automation and control. Comprising 48 chapters and the contributions of 74 leading experts from industry and academia, the Embedded Systems Handbook, Second Edition, presents a comprehensive view of embedded systems, their design, verification, networking, and applications. The contributors, directly involved in the creation and evolution of the ideas and technologies presented, offer tutorials, research surveys, and technology overviews exploring new developments, deployments, and trends. To accommodate the tremendous growth in the field, the handbook is now divided into two volumes. New in This Edition: Processors for embedded systems; Processor-centric architecture; description languages; Networked embedded systems in the automotive and industrial automation fields; Wireless embedded systems; Embedded Systems Design and Verification. Volume I of the handbook is divided into three sections. It begins with a brief introduction to embedded systems design and verification. The book then provides a comprehensive overview of embedded processors and various aspects of system-on-chip and FPGA as well as solutions to design challenges. The final section explores power-aware embedded computing design issues specific to secure embedded systems and web services for embedded devices. Networked Embedded Systems. Volume II focuses on selected application areas of networked embedded systems. It covers automotive, field industrial automation, building automation, and wireless sensor networks. This volume highlights implementations in fast-evolving areas which have not received proper coverage in other publications. Reflecting the unique functional requirements of different application areas, the contributors discuss inter-node communication aspects in the context of specific applications of networked embedded systems.

SystemC: From the Ground Up David C. Black, Jack Donovan, 2007-05-08 SystemC provides a robust set of extensions to C that enables rapid development of complex hardware/software systems. This book focuses on the practical uses of the language for modeling real systems. The wealth of examples and downloadable code

methodically guide the reader through the finer points of the SystemC language This work provides A step by step build up of syntax NEW features of SystemC 2 1 Code examples for each concept Many resource references Coding styles and guidelines Over 52 downloadable code examples over 8 000 lines Exercises throughout the book How SystemC fits into the system design methodology Why features are as they are Well known consultants in the EDA industry both David Black and Jack Donovan have been involved in the adoption and teaching of new technologies and methodologies for a combined total of 42 years Recently they jointly founded a consultancy Eklectic Ally focused on helping companies adopt SystemC methodologies

Digital Design (VHDL) Peter J. Ashenden, 2007-10-24 Digital Design An Embedded Systems Approach Using VHDL provides a foundation in digital design for students in computer engineering electrical engineering and computer science courses It takes an up to date and modern approach of presenting digital logic design as an activity in a larger systems design context Rather than focus on aspects of digital design that have little relevance in a realistic design context this book concentrates on modern and evolving knowledge and design skills Hardware description language HDL based design and verification is emphasized VHDL examples are used extensively throughout By treating digital logic as part of embedded systems design this book provides an understanding of the hardware needed in the analysis and design of systems comprising both hardware and software components Includes a Web site with links to vendor tools labs and tutorials Presents digital logic design as an activity in a larger systems design context Features extensive use of VHDL examples to demonstrate HDL hardware description language usage at the abstract behavioural level and register transfer level as well as for low level verification and verification environments Includes worked examples throughout to enhance the reader's understanding and retention of the material Companion Web site includes links to tools for FPGA design from Synplicity Mentor Graphics and Xilinx VHDL source code for all the examples in the book lecture slides laboratory projects and solutions to exercises

From ASICs to SOCs Farzad Nekoogar, Faranak Nekoogar, 2003 From ASICs to SOCs A Practical Approach by Farzad Nekoogar and Faranak Nekoogar covers the techniques principles and everyday realities of designing ASICs and SOCs Material includes current issues in the field front end and back end designs integration of IPs on SOC designs and low power design techniques and methodologies Appropriate for practicing chip designers as well as graduate students in electrical engineering

Integrated Circuit and System Design Enrico Macii, Vassilis Paliouras, Odysseas Koufopavlou, 2004-09-07 This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation PATMOS 2004 held in Santorini Greece in September 2004 The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted The papers are organized in topical sections on buses and communication circuits and devices low power issues architectures asynchronous circuits systems design interconnect and physical design security and safety low power processing digital design and modeling and simulation

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation

Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing

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