Models for Large Integrated Circuits

Patrick Dewilde Zhen-Qiu Ning

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Models For Large Integrated Circuits

Enrico Macii, Vassilis Paliouras, Odysseas Koufopavlou

Models For Large Integrated Circuits:

Models for Large Integrated Circuits Patrick DeWilde, Zhen-Qiu Ning, 2012-01-04 A modern microelectronic circuit can be compared to a large construction a large city on a very small area A memory chip a DRAM may have up to 64 million bit locations on a surface of a few square centimeters Each new generation of integrated circuit generations are measured by factors of four in overall complexity requires a substantial increase in density from the current technology added precision a decrease of the size of geometric features and an increase in the total usable surface. The microelectronic industry has set the trend Ultra large funds have been invested in the construction of new plants to produce the ultra large scale circuits with utmost precision under the most severe conditions. The decrease in feature size to submicrons 0.7 micron is quickly becoming availabl does not only bring technological problems New design problems arise as well The elements from which microelectronic circuits are build transistors and interconnects have different shape and behave differently than before Phenomena that could be neglected in a four micron technology such as the non uniformity of the doping profile in a transistor or the mutual capacitance between two wires now play an important role in circuit design This situation does not make the life of the electronic designer easier he has to take many more parasitic effects into account up to the point that his ideal design will not function as originally planned **Compact Models for Integrated Circuit Design Samar K.** Saha, 2018-09-03 Compact Models for Integrated Circuit Design Conventional Transistors and Beyond provides a modern treatise on compact models for circuit computer aided design CAD Written by an author with more than 25 years of industry experience in semiconductor processes devices and circuit CAD and more than 10 years of academic experience in teaching compact modeling courses this first of its kind book on compact SPICE models for very large scale integrated VLSI chip design offers a balanced presentation of compact modeling crucial for addressing current modeling challenges and understanding new models for emerging devices Starting from basic semiconductor physics and covering state of the art device regimes from conventional micron to nanometer this text Presents industry standard models for bipolar junction transistors BJTs metal oxide semiconductor MOS field effect transistors FETs FinFETs and tunnel field effect transistors TFETs along with statistical MOS models Discusses the major issue of process variability which severely impacts device and circuit performance in advanced technologies and requires statistical compact models Promotes further research of the evolution and development of compact models for VLSI circuit design and analysis Supplies fundamental and practical knowledge necessary for efficient integrated circuit IC design using nanoscale devices Includes exercise problems at the end of each chapter and extensive references at the end of the book Compact Models for Integrated Circuit Design Conventional Transistors and Beyond is intended for senior undergraduate and graduate courses in electrical and electronics engineering as well as for researchers and practitioners working in the area of electron devices However even those unfamiliar with semiconductor physics gain a solid grasp of compact modeling concepts from this book **Integrated Circuit and System**

Design. Power and Timing Modeling, Optimization and Simulation Johan Vounckx, Nadine Azemard, Philippe Maurine, 2006-09-07 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation José Monteiro, Rene van Leuken, 2010-02-18 This book constitutes the thoroughly refereed post conference proceedings of 19th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2009 featuring Integrated Circuit and System Design held in Delft The Netherlands during September 9 11 2009 The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions The papers are organized in topical sections on variability statistical timing circuit level techniques power management low power circuits technology system level techniques power timing optimization techniques self timed circuits low power circuit analysis optimization and low power design studies **Integrated Circuit and System Design. Power** and Timing Modeling, Optimization and Simulation Nadine Azemard, 2007-08-21 This volume features the refereed proceedings of the 17th International Workshop on Power and Timing Modeling Optimization and Simulation Papers cover high level design low power design techniques low power analog circuits statistical static timing analysis power modeling and optimization low power routing optimization security and asynchronous design low power applications modeling and Optoelectronic Integrated Circuit Design and Device Modeling Jianjun Gao, 2011-09-19 In optimization and more Optoelectronic Integrated Circuit Design and Device Modeling Professor Jianjun Gao introduces the fundamentals and modeling techniques of optoelectronic devices used in high speed optical transmission systems Gao covers electronic circuit elements such as FET HBT MOSFET as well as design techniques for advanced optical transmitter and receiver front end circuits The book includes an overview of optical communication systems and computer aided optoelectronic IC design before going over the basic concept of laser diodes This is followed by modeling and parameter extraction techniques of lasers and photodiodes Gao covers high speed electronic semiconductor devices optical transmitter design and optical receiver design in the final three chapters Addresses a gap within the rapidly growing area of transmitter and receiver modeling in OEICs Explains diode physics before device modeling helping readers understand their equivalent circuit models Provides comprehensive explanations for E O and O E conversions done with laser and photodiodes Covers an extensive range of devices for high speed applications Accessible for students new to microwaves Presentation slides available for instructor use This book is primarily aimed at practicing engineers researchers and post graduates in the areas of RF microwaves IC design photonics and lasers and solid state devices The book is also a strong supplement for senior undergraduates taking courses

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courses on manufacturing Integrated Circuit Design. Power and Timing Modeling, Optimization and Simulation Bertrand Hochet, Antonio J. Acosta, 2002-08-28 This book constitutes the refereed proceedings of the 12th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2002 held in Seville Spain in September 2002 The 37 revised full papers and 12 poster papers presented were carefully reviewed and selected from numerous submissions The papers are organized in topical sections on arithmetics low level modeling and characterization asynchronous and adiabatic techniques CAD tools and algorithms timing gate level modeling and design and communications modeling and activity Modeling, Simulation, and Optimization of Integrated Circuits K. Antreich, R. Bulirsch, A. Gilg, P. Rentrop, 2012-12-06 In November 2001 the Mathematical Research Center at Oberwolfach Germany hosted the third Conference on Mathematical Models and Numerical Simulation in Electronic Industry It brought together researchers in mathematics electrical engineering and scientists working in industry The contributions to this volume try to bridge the gap between basic and applied mathematics research in electrical engineering and the needs of industry International Conference on Computing in High Energy Physics '95, 1996 CHEP Computing in High Energy Physics is the largest international meeting of the communities of High Energy Physics Computing Science and the Computing Industry The sixth conference in this series was held in Rio de Janeiro Brazil in September 1995 The focus of the conference was Computing for the next Millennium High Energy Physics is at a point where major changes in the way data acquisition and computing problems are addressed will be called for in the high energy physics programs of the year 2000 and beyond The conference covered a wide spectrum of topics including Data Access Storage and Analysis Data Acquisition and Triggering Worldwide Collaboration and Networking Tools Languages and Software Development Environments and special purpose processing systems. The papers presented both recent progress and radical approaches to computing problems as candidates for the basis of future computing in the field of high energy physics Provided by publisher Model Reduction for Circuit Simulation Peter Benner, Michael Hinze, E. Jan W. ter Maten, 2011-03-25 Simulation based on mathematical models plays a major role in computer aided design of integrated circuits ICs Decreasing structure sizes increasing packing densities and driving frequencies require the use of refined mathematical models and to take into account secondary parasitic effects This leads to very high dimensional problems which nowadays require simulation times too large for the short time to market demands in industry Modern Model Order Reduction MOR techniques present a way out of this dilemma in providing surrogate models which keep the main characteristics of the device while requiring a significantly lower simulation time than the full model With Model Reduction for Circuit Simulation we survey the state of the art in the challenging research field of MOR for ICs and also address its future research directions Special emphasis is taken on aspects stemming from miniturisations to the nano scale Contributions cover complexity reduction using e g balanced truncation Krylov techniques or POD approaches For semiconductor applications a focus is on generalising current techniques to differential algebraic

equations on including design parameters on preserving stability and on including nonlinearity by means of piecewise linearisations along solution trajectories TPWL and interpolation techniques for nonlinear parts Furthermore the influence of interconnects and power grids on the physical properties of the device is considered and also top down system design approaches in which detailed block descriptions are combined with behavioral models Further topics consider MOR and the combination of approaches from optimisation and statistics and the inclusion of PDE models with emphasis on MOR for the resulting partial differential algebraic systems. The methods which currently are being developed have also relevance in other application areas such as mechanical multibody systems and systems arising in chemistry and to biology The current number of books in the area of MOR for ICs is very limited so that this volume helps to fill a gap in providing the state of the art material and to stimulate further research in this area of MOR Model Reduction for Circuit Simulation also reflects and documents the vivid interaction between three active research projects in this area namely the EU Marie Curie Action ToK project O MOORE NICE members in Belgium The Netherlands and Germany the EU Marie Curie Action RTN project COMSON members in The Netherlands Italy Germany and Romania and the German federal project System reduction in nano electronics SyreNe Three-Dimensional Integrated Circuit Design Vasilis F. Pavlidis, Ioannis Savidis, Eby G. Friedman, 2017-07-04 Three Dimensional Integrated Circuit Design Second Eition expands the original with more than twice as much new content adding the latest developments in circuit models temperature considerations power management memory issues and heterogeneous integration 3 D IC experts Pavlidis Savidis and Friedman cover the full product development cycle throughout the book emphasizing not only physical design but also algorithms and system level considerations to increase speed while conserving energy A handy comprehensive reference or a practical design guide this book provides effective solutions to specific challenging problems concerning the design of three dimensional integrated circuits Expanded with new chapters and updates throughout based on the latest research in 3 D integration Manufacturing techniques for 3 D ICs with TSVs Electrical modeling and closed form expressions of through silicon vias Substrate noise coupling in heterogeneous 3 D ICs Design of 3 D ICs with inductive links Synchronization in 3 D ICs Variation effects on 3 D ICs Correlation of WID variations for intra tier buffers and wires Offers practical guidance on designing 3 D heterogeneous systems Provides power delivery of 3 D ICs Demonstrates the use of 3 D ICs within heterogeneous systems that include a variety of materials devices processors GPU CPU integration and more Provides experimental case studies in power delivery synchronization and thermal characterization Technology Computer Aided Design for Si, SiGe and GaAs Integrated Circuits G.A. Armstrong, C.K. Maiti, 2007-11-30 The first book to deal with a broad spectrum of process and device design and modeling issues related to semiconductor devices bridging the gap between device modelling and process design using TCAD Presents a comprehensive perspective of emerging fields and covers topics ranging from materials to fabrication devices modelling and applications Aimed at research and development engineers and scientists involved in microelectronics

technology and device design via Technology CAD and TCAD engineers and developers **Integrated Circuit and System** Design. Power and Timing Modeling, Optimization and Simulation Jose L. Ayala, Braulio Garcia-Camara, Manuel Prieto, Martino Ruggiero, Gilles Sicard, 2011-09-15 This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design PATMOS 2011 held in Madrid Spain in September 2011 The 34 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization Integrated Circuit and System Design Enrico Macii, Vassilis Paliouras, Odysseas Koufopavlou, 2004-09-07 This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation PATMOS 2004 held in Santorini Greece in September 2004 The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted The papers are organized in topical sections on buses and communication circuits and devices low power issues architectures asynchronous circuits systems design interconnect and physical design security and safety low power processing digital design and modeling and simulation

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