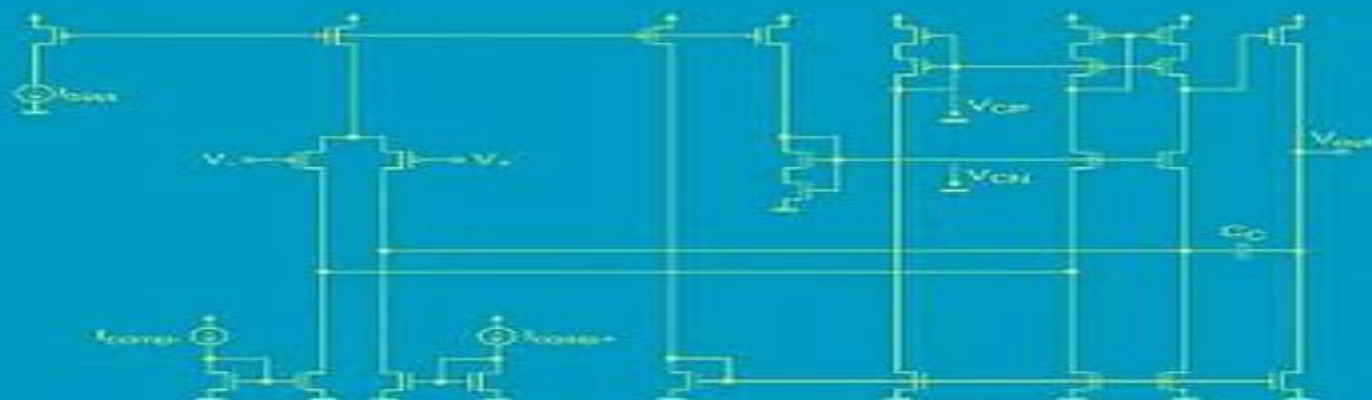


METHODOLOGY FOR THE DIGITAL CALIBRATION OF ANALOG CIRCUITS AND SYSTEMS

with Case Studies

Marc Pastre and Maher Kayal



Methodology For The Digital Calibration Of Analog Circuits And Systems With Case Stuidies

Roman Wölfel



Methodology For The Digital Calibration Of Analog Circuits And Systems With Case Studies:

Methodology for the Digital Calibration of Analog Circuits and Systems Marc Pastre, Maher Kayal, 2006 Methodology for the Digital Calibration of Analog Circuits and Systems shows how to relax the extreme design constraints in analog circuits allowing the realization of high precision systems even with low performance components A complete methodology is proposed and three applications are detailed To start with an in depth analysis of existing compensation techniques for analog circuit imperfections is carried out The M 2 M sub binary digital to analog converter is thoroughly studied and the use of this very low area circuit in conjunction with a successive approximations algorithm for digital compensation is described A complete methodology based on this compensation circuit and algorithm is then proposed The detection and correction of analog circuit imperfections is studied and a simulation tool allowing the transparent simulation of analog circuits with automatic compensation blocks is introduced The first application shows how the sub binary M 2 M structure can be employed as a conventional digital to analog converter if two calibration and radix conversion algorithms are implemented The second application a SOI 1T DRAM is then presented A digital algorithm chooses a suitable reference value that compensates several circuit imperfections together from the sense amplifier offset to the dispersion of the memory read currents The third application is the calibration of the sensitivity of a current measurement microsystem based on a Hall magnetic field sensor Using a variant of the chopper modulation the spinning current technique combined with a second modulation of a reference signal the sensitivity of the complete system is continuously measured without interrupting normal operation A thermal drift lower than 50 ppm C is achieved which is 6 to 10 times less than in state of the art implementations Furthermore the calibration technique also compensates drifts due to mechanical stresses and ageing

Analog Circuit Design Techniques at 0.5V Shouri Chatterjee, K.P. Pun, Nebojša Stanic, Yannis Tsividis, Peter Kinget, 2010-04-02 Analog design at ultra low supply voltages is an important challenge for the semiconductor research community and industry Analog Circuit Design Techniques at 0.5V covers challenges for the design of MOS analog and RF circuits at a 0.5 V power supply voltage All design techniques presented are true low voltage techniques all nodes in the circuits are within the power supply rails The circuit implementations of body and gate input fully differential amplifiers are also discussed These building blocks enable us to build continuous time filters track and hold circuits and continuous time sigma delta modulators Current books on low voltage analog design typically cover techniques for supply voltages down to approximately 1V This book presents novel ideas and results for operation from much lower supply voltages and the techniques presented are basic circuit techniques that are widely applicable beyond the scope of the presented examples Analog Circuit Design Techniques at 0.5V is written for analog circuit designers and researchers as well as graduate students studying semiconductors and integrated circuit design

CMOS Current-Mode Circuits for Data Communications Fei Yuan, 2007-04-26 Current mode circuits where information is represented by the branch currents of the circuits rather than the nodal voltages as of voltage mode

circuits possess many unique and attractive characteristics over their voltage mode counterparts including a small nodal time constant high current swing in the presence of a low supply voltage reduced distortion a low input impedance a high output impedance less sensitive to switching noise and better ESD immunity CMOS current mode circuits have found increasing applications in telecommunication systems instrumentation analog signal processing multiprocessors high speed computer interfaces and the backplane of complex electronic systems This book deals with the analysis and design of continuous time CMOS current mode circuits for data communications over wire channels CMOS current mode sampled data networks such as switch current circuits and current mode logic circuits are excluded The book is organized as follows Chapter 1 examines the distinct characteristics of ideal voltage mode and current mode circuits The topology duality of these two classes of circuits is investigated using the concept of inter reciprocity and adjoint network A critical comparison of the input and output impedances bandwidth slew rate propagation delay signal swing supply voltage sensitivity and ESD sensitivity of voltage mode and current mode circuits is provided Chapter 2 investigates design techniques that improve the performance of low voltage current mode circuits including input impedance reduction output impedance boosting bandwidth enhancement mismatch compensation power consumption reduction and swing improvement Chapter 3 investigates the modeling of wire channels

Advanced Design Techniques for RF Power Amplifiers Anna N. Rudiakova, Vladimir Krizhanovski, 2006-09-09 Advanced Design Techniques for RF Power Amplifiers main aim is to provide the reader with a deep analysis of theoretical aspects modelling and design strategies of RF high efficiency power amplifiers Advanced Design Techniques for RF Power Amplifiers begins with an analytical review of current state of the problem Then it moves to the theoretical analysis of BJT class F power amplifier near transition frequency and presents the necessary realization conditions The next part concerns the practical verification and demonstration of the theoretical results It is followed by the part devoted to the output networks of high efficiency power amplifiers The novel type of photonic band gap structure providing improved characteristics both in the pass and stop bands is proposed Finally the fifth harmonic peaking class F power amplifier design based on the above structure is presented

Design of High Voltage xDSL Line Drivers in Standard CMOS Bert Serneels, Michiel Steyaert, 2008-01-08 Design of high voltage xDSL line drivers in standard CMOS fits in the quest for highly efficient fully integrated xDSL modems for central office applications The book focusses on the line driver the most demanding building block of the xDSL modem for lowering power To reduce the cost the cheapest technology is selected standard CMOS without any extra process options to increase the nominal supply voltage The emphasis lies on the analysis design and implementation of high voltage highly efficient line drivers in mainstream CMOS Design of high voltage xDSL line drivers in standard CMOS covers the total design flow of monolithic CMOS high voltage circuits The book is essential reading for analog design engineers and researchers in the field and is also suitable as a text book for an advanced course on the subject

Analog-Baseband Architectures and Circuits for Multistandard and Low-Voltage Wireless

Transceivers Pui-In Mak, Ben U Seng Pan, Rui Paulo Martins, 2007-09-07 This book presents architectural and circuit techniques for wireless transceivers to achieve multistandard and low voltage compliance It provides an up to date survey and detailed study of the state of the art transceivers for modern single and multi purpose wireless communication systems The book includes comprehensive analysis and design of multimode reconfigurable receivers and transmitters for an efficient multistandard compliance

Precision Temperature Sensors in CMOS Technology Micheal A.P. Pertijs, Johan Huijsing, 2006-12-06 The low cost and direct digital output of CMOS smart temperature sensors are important advantages compared to conventional temperature sensors This book addresses the main problem that nevertheless prevents widespread plication of CMOS smart temperature sensors their relatively poor absolute accuracy Several new techniques are introduced to improve this accuracy The effectiveness of these techniques is demonstrated using three prototypes The nal prototype achieves an inaccuracy of 0.1 °C over the military temperature range which is a significant improvement in the state of the art Since smart temperature sensors have been the subject of academic and industrial research for more than two decades an overview of existing knowledge and techniques is also provided throughout the book In this introductory chapter the motivation and objectives of this work are scribed This is followed by a review of the basic operating principles of CMOS smart temperature sensors and a brief overview of previous work The challenges are then described that need to be met in order to improve the accuracy of CMOS smart temperature sensors while maintaining their cost advantage Finally the structure of the rest of the book is introduced

Full-Chip Nanometer Routing Techniques Tsung-Yi Ho, Yao-Wen Chang, Sao-Jie Chen, 2007-08-30 At 90 nm wires account for nearly 75% of the total delay in a circuit Even more insidious however is that among nearly 40% of these nets more than 50% of their total net capacitance are attributed to the cross coupling capacitance between neighboring signals At this point a new design and optimization paradigm based on real wires is required Nanometer routers must prevent and correct these effects on the fly in order to reach timing closure From a manufacturability standpoint nanometer routers must explicitly deal with the ever increasing design complexity and be capable of adapting to the constraint requirements of timing signal integrity process antenna effect and new interconnect architecture such as X architecture In the nanometer era we must look into new generation routing technologies that combine high performance and capacity with the integration of congestion timing SI prevention and DFM algorithms as the best means of getting to design closure quickly In this book we present a novel multilevel full chip router namely mSIGMA for SIGNAL integrity and MANufacturability optimization And these routing technologies will ensure faster time to market and time to profitability

Sigma Delta A/D Conversion for Signal Conditioning Kathleen Philips, Arthur H.M. van Roermund, 2006-05-05 1.1 Background Moore's Law predicts a decrease by a factor of two in the feature size of CMOS technology every three years and has been valid for years It implies a doubling of the era tion speed and a four times higher transistor count per unit of area every three years The combination leads to an eight times higher processing capability per

unit of area This on going miniaturization allows the integration of complex electronic systems with millions of transistors Very Large Scale Integration and enables the integration of electronic systems An electronic system A generic picture of an integrated electronic system is shown in g 1 1 The heart of the system is the signal processing core This core supports a wide variety of functions such as customization and programmability of multiple applications channel coding the definition of the user interface etc These functions are enabled by DSP a controller CPU and various blocks of memory In advanced ICs these blocks provide almost all signal processing and usually dominate in the overall power and area consumption of integrated systems The huge data rates involved require high speed busses for communication between these blocks A power management unit fuels the system by providing the appropriate supply voltages and currents

RF Power Amplifiers for Mobile Communications Patrick Reynaert, Michiel Steyaert, 2006-11-18 This book tackles both high efficiency and high linearity power amplifier PA design in low voltage CMOS With its emphasis on theory design and implementation the book offers a guide for those actively involved in the design of fully integrated CMOS wireless transceivers Offering mathematical background as well as intuitive insight the book is essential reading for RF design engineers and researchers and is also suitable as a text book

CMOS Single Chip Fast Frequency Hopping Synthesizers for Wireless Multi-Gigahertz Applications Taoufik Bourdi, Izzet Kale, 2007-03-06 In this book the authors outline detailed design methodology for fast frequency hopping synthesizers for RF and wireless communications applications There is great emphasis on fractional N delta sigma based phase locked loops from specifications system analysis and architecture planning to circuit design and silicon implementation The developed techniques in the book can help in designing very low noise high speed fractional N frequency synthesizers

CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom Rocío Río Fernández, Fernando Medeiro Hidalgo, Belén Pérez Verdú, José Manuel Rosa Utrera, Ángel Rodríguez-Vázquez, 2006-09-03 Institutional book not really for bookstore catalogue The book contains valuable information structured to provide insight on how to design SC sigma delta modulators It presents architectures circuits models methods and practical considerations for the design of high performance low pass switched capacitor SC sigma delta A/D interfaces for mixed signal CMOS ASICs The main focus of the book is on cascade architectures It differs from other books in the complete in depth coverage of SC circuit errors

Broadband Opto-Electrical Receivers in Standard CMOS Carolien Hermans, Michiel Steyaert, 2007-06-13 Broadband Opto Electrical Receivers in Standard CMOS starts from the basic fundamentals necessary for the design of optoelectronic interface circuits The book continues with an in depth analysis of the photodiode transimpedance amplifier TIA and limiting amplifier LA To thoroughly understand the light detection mechanisms in silicon first a one dimensional and second a two dimensional model is developed Analytical design equations are derived to guide the design of the amplifying circuits For the TIA the focus is on the sensitivity speed trade off For the LA a high gain bandwidth is pursued Several practical design examples reveal the subtleties and challenges encountered during the design of high performance analog

circuits Broadband Opto Electrical Receivers in Standard CMOS covers the total design flow of monolithic CMOS optical receivers All material is experimentally verified with several CMOS implementations with ultimately a fully integrated Gbit s optical receiver front end including photodiode TIA and LA

Switched-Capacitor Techniques for High-Accuracy Filter and ADC Design Patrick J. Quinn, Arthur H.M. van Roermund, 2007-07-20 This book proposes alternative switched capacitor techniques which allow the achievement of higher intrinsic analogue functional accuracy than previously possible in such application areas as analogue filter and ADC design The validity of the concepts developed and analyzed in Switched Capacitor Techniques for High Accuracy Filter and ADC Design has been demonstrated in practice with the design of CMOS SC bandpass filters and algorithmic ADC stages

Low-Frequency Noise in Advanced MOS Devices Martin Haartman, Mikael Östling, 2007-08-23 Low Frequency Noise in Advanced CMOS Devices begins with an introduction to noise describing the fundamental noise sources and basic circuit analysis The characterization of low frequency noise is discussed in detail and useful practical advice is given The various theoretical and compact low frequency $1/f$ noise models in MOS transistors are treated extensively providing an in depth understanding of the low frequency noise mechanisms and the potential sources of the noise in MOS transistors Advanced CMOS technology including nanometer scaled devices strained Si SiGe SOI high k gate dielectrics multiple gates and metal gates are discussed from a low frequency noise point of view Some of the most recent publications and conference presentations are included in order to give the very latest view on the topics The book ends with an introduction to noise in analog RF circuits and describes how the low frequency noise can affect these circuits

CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications Paul Muller, Yusuf Leblebici, 2007-10-29 In the world of optical data communications this book will be an absolute must read It focuses on optical communications for short and very short distance applications and discusses the monolithic integration of optical receivers with processing elements in standard CMOS technologies What's more it provides the reader with the necessary background knowledge to fully understand the trade offs in short distance communication receiver design and presents the key issues to be addressed in the development of such receivers in CMOS technologies Moreover novel design approaches are presented

Adaptive Multi-Standard RF Front-Ends Vojkan Vidojkovic, J. van der Tang, Arjan Leeuwenburgh, Arthur H.M. van Roermund, 2008-02-07 In this information era people are living in a society in which processing and exchange of information are vital for their existence Two major issues in such society which are related to flow and exchange of information are connectivity and mobility On one hand computers and Internet provide connectivity and allow communication as well as fast access to large amounts of information On the other hand wireless technologies bring mobility People can move and still be able to communicate and have access to various kind of information Therefore the functioning of an information society is unthinkable without the use of computers Internet and wireless technologies The expectations are that in the future they will merge into a unique system for communication access to information as well as their exchange and processing The era of

wireless communications started in 1901 when Guglielmo Marconi successfully transmitted radio signals across the Atlantic Ocean. From that moment up to now, wireless communications experienced explosive growth and became the fastest growing field in the engineering world. Pushed by customer requirements, new wireless technologies have been emerging very fast. Each new generation of wireless technologies has brought new features and more complexity. Pushed by market forces to reduce costs, the semiconductor industry has provided new technologies for solid state circuits implementation. Fortunately, at the same time, with the cost reduction, the performance of new technologies has been improving.

Wide-Bandwidth High Dynamic Range D/A Converters Konstantinos Doris, Arthur H.M. van Roermund, Domine Leenaerts, 2006-01-12

IGH SPEED Digital to Analog D/A converters are essential components in digital communication systems, providing the necessary conversion of signals encoding information in bits to signals encoding information in their amplitude vs. time domain characteristics. In general, they are parts of a larger system, the interface, which consists of several signal conditioning circuits. Dependent on where the converter is located within the chain of circuits in the interface, signal processing operations are partitioned into those realized with digital techniques and those with analog. The rapid evolution of CMOS technology has established implicit and explicit trends related to the interface and, in particular, to the D/A converter. The implicit relationship comes via the growth of digital systems. First, it is a global trend with respect to all interface circuits that increasing operating frequencies of digital systems place a similar demand for the interface circuits. The second trend takes place locally within the interface. Initially, the D/A converter was placed at the beginning of the interface chain, and all signal conditioning was implemented in the analog domain after the D/A conversion. The increasing flexibility and robustness of digital signal processing shifted the D/A converter closer to the end point of the chain, where the demands for high quality, high frequency operation are very high.

Analog Circuit Design for Process Variation-Resilient Systems-on-a-Chip Marvin Onabajo, Jose Silva-Martinez, 2012-03-08

This book describes several techniques to address variation-related design challenges for analog blocks in mixed-signal systems on-chip. The methods presented are results from recent research works involving receiver front-end circuits, baseband filter linearization, and data conversion. These circuit-level techniques are described with their relationships to emerging system-level calibration approaches to tune the performances of analog circuits with digital assistance or control. Coverage also includes a strategy to utilize on-chip temperature sensors to measure the signal power and linearity characteristics of analog RF circuits, as demonstrated by test-chip measurements. Describes a variety of variation-tolerant analog circuit design examples, including from RF front-ends, high-performance ADCs, and baseband filters. Includes built-in testing techniques linked to current industrial trends. Balances digitally assisted performance tuning with analog performance tuning and mismatch reduction approaches. Describes theoretical concepts as well as experimental results for test chips designed with variation-aware techniques.

Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design Fakhfakh, Mourad, Tlelo-Cuautle, Esteban, Fino, Maria

Helena,2014-10-31 Improving the performance of existing technologies has always been a focal practice in the development of computational systems However as circuitry is becoming more complex conventional techniques are becoming outdated and new research methodologies are being implemented by designers Performance Optimization Techniques in Analog Mixed Signal and Radio Frequency Circuit Design features recent advances in the engineering of integrated systems with prominence placed on methods for maximizing the functionality of these systems This book emphasizes prospective trends in the field and is an essential reference source for researchers practitioners engineers and technology designers interested in emerging research and techniques in the performance optimization of different circuit designs

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