

# Selective probing method using SEM for inline electrical inspection of semiconductor devices

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## Introduction

Continuity of post-BC integrated semiconductor devices is becoming leading to detect and inspect defects that cannot be detected by traditional top-view-based inline electrical inspection. These defects are often only detected at the end of the line of the device. To detect process feedback that an inline inspection line is placed. Measuring electrical properties is essential for detecting invisible defects. By measuring electrical properties, it is possible to evaluate defects such as poor contact, leakage current and dimensional variations in buried layers. Therefore, Hitachi has developed a selective probing method to detect defects in process using transient signals of SEM.



Fig. 1: Device development process with inline E-test

## Selective probing method

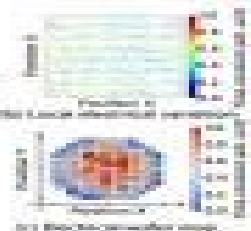
To estimate electrical properties, the selective probing method targets signal with defined electron beams and measures the transient signals of electrical capacitance elements (ECC). The transient signals are dynamic voltage response (VCC) which reflects dynamics on localized semiconductor columns with pin electrical properties. Therefore, transient features in the signal contain at least one signal, which enables the measurement of the device's resistance and capacitance. The distribution of electrical characteristics, yield of factors and the basic electrical parameters within inspection can be evaluated by using these features in electrical circuit.



Fig. 2: Selective probing method



Fig. 3: Selective probing output



## Electrical inspection

An example of electrical inspection process is presented with selective probing method. The transient signals of electrical capacitance elements (ECC) are measured with defined electron beams and measure the transient signals of electrical capacitance elements (ECC). The transient signals are dynamic voltage response (VCC) which reflects dynamics on localized semiconductor columns with pin electrical properties. Therefore, transient features in the signal contain at least one signal, which enables the measurement of the device's resistance and capacitance. The distribution of electrical characteristics, yield of factors and the basic electrical parameters within inspection can be evaluated by using these features in electrical circuit.

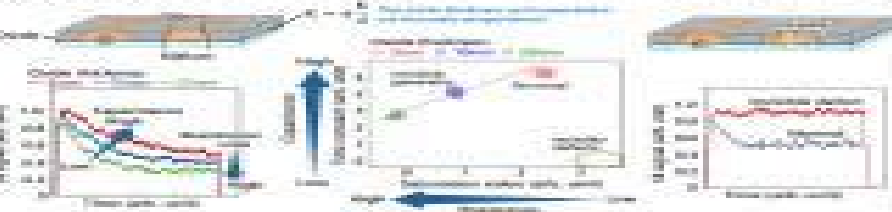


Fig. 4: Transient analysis for impedance distribution

## Result

To evaluate the electrical properties of the device, the transient signals of electrical capacitance elements (ECC) are measured with defined electron beams and measure the transient signals of electrical capacitance elements (ECC). The transient signals are dynamic voltage response (VCC) which reflects dynamics on localized semiconductor columns with pin electrical properties. Therefore, transient features in the signal contain at least one signal, which enables the measurement of the device's resistance and capacitance. The distribution of electrical characteristics, yield of factors and the basic electrical parameters within inspection can be evaluated by using these features in electrical circuit.



Fig. 5: Transient features of ECC for electrical inspection

## Conclusion

The developed selective probing method measuring transient signals of recorded electrical circuit for electrical properties of semiconductor devices. The measured transient signals of the device, including the following:  
- The transient signals can be measured with the transient signals.  
- Marginal malfunctions that cannot be identified in the top view can be exposed.

## References

- [1] Hitachi High-Technologies America, Inc., 10000 North Central Expressway, Santa Fe, New Mexico 87504
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Fig. 6: Transient signals of the device differences

The selective probing method can detect "invisible" defects buried in the buried layers through transient signals.

# Semiconductor Devices Spie Vol 2733

**Raffaela Di Napoli**



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[illegible]

device design by defining optimal device structures and manipulating impurity profiles to obtain optimal control of the carrier flow through the device. This becomes increasingly difficult as the device scale becomes smaller and smaller. Since the introduction of integrated circuits the number of individual transistors on a single chip has doubled approximately every three years. As the number of devices has grown the critical dimension of the smallest feature such as a gate length which is related to the transport length defining the channel has consequently declined. The reduction of this design rule proceeds approximately by a factor of 1.4 each generation which means we will be using 0.1015  $\mu\text{m}$  rules for the 4 Gb chips a decade from now. If we continue this extrapolation current technology will require 30 nm design rules and a cell 3.2 size.

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