

Low Power CMOS VLSI Design: Implementation of Comparator Circuits Using Novel Technique

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Abstract -- Low power has emerged as a principal theme in today's electronic industry. Reduction of power consumption makes a device more reliable and efficient. As the demand of portable consumer electronics increases, and the size of the chip decreases, challenges towards the power dissipated are induced. Complementary Metal Oxide Semiconductor (CMOS) logic styles are best known for dissipating less energy or low power. The Proposed topology aims to design comparator logic circuits with different logic styles such as conventional CMOS, dynamic CMOS and domino CMOS. Initially, a single bit comparator will be designed and its functionality will be verified with all the three kinds of styles mentioned above. Using this design, by connecting them in a cascaded fashion, higher bit comparator circuits (4-bit and 8-bit) shall be obtained and a comparison will be drawn between the existing technology and the proposed design.

Keywords: CMOS logic, Comparators, Dynamic logic, dynamic CMOS, Low power

I. INTRODUCTION

A comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +ve VP, the input of the comparator is at a greater potential than the -ve VN, input, the output of the comparator is a logic 1, where as if the +ve input is at a potential less than the -ve input, the output of the comparator is at logic 0.

Figure 1. Comparator Operations.

If $V_P < V_N$ then $V_O = V_{SS} = \text{logic } 0$.
If $V_P > V_N$ then $V_O = V_{DD} = \text{logic } 1$.

II. LITERATURE REVIEW

According to Moore's Law, since the number of transistors integrated in a chip doubles once in every 18 months, thus, the role of circuit designers become very crucial. Decades ago, Speed and area were the important constraints and not power because the number of transistors involved in a design were quite less around

hundreds or thousands, but in the present scenario, as the complexity of the chips increase, millions of transistors are integrated in order to achieve the task with more functionalities and features. Hence, the power Dissipation of the overall chip or product is an extremely large value and has to be reduced significantly using suitable design techniques. This can be achieved by a number of ways such as reducing the number of transistors i.e. modifying the design which occupies a lesser number of transistors for the same functionality.

The main objective of this paper is to implement the higher bit comparator circuits with fewer transistors so that the total power dissipation will be reduced. We have implemented comparator circuits using conventional CMOS (Complementary Metal Oxide Semiconductor) and dynamic CMOS logic styles. Conventional CMOS technology implementation offers low power because of the nmos and pmos transistors behavior. While the pull

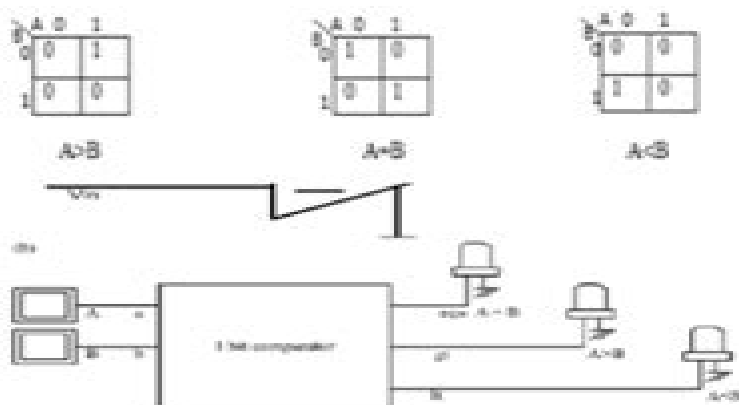


Figure 1.(a) Karnaugh map for a one – bit comparator.
Figure (b). Block diagram of a One – bit comparator.

up network is on, the pull down network is off and vice versa. So, the static power dissipation is ideally zero.

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Table of Contents Low Power Cmos Design

1. Understanding the eBook Low Power Cmos Design
 - The Rise of Digital Reading Low Power Cmos Design
 - Advantages of eBooks Over Traditional Books
2. Identifying Low Power Cmos Design
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Low Power Cmos Design
 - User-Friendly Interface
4. Exploring eBook Recommendations from Low Power Cmos Design
 - Personalized Recommendations
 - Low Power Cmos Design User Reviews and Ratings
 - Low Power Cmos Design and Bestseller Lists
5. Accessing Low Power Cmos Design Free and Paid eBooks

- Low Power Cmos Design Public Domain eBooks
- Low Power Cmos Design eBook Subscription Services
- Low Power Cmos Design Budget-Friendly Options
- 6. Navigating Low Power Cmos Design eBook Formats
 - ePub, PDF, MOBI, and More
 - Low Power Cmos Design Compatibility with Devices
 - Low Power Cmos Design Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Low Power Cmos Design
 - Highlighting and Note-Taking Low Power Cmos Design
 - Interactive Elements Low Power Cmos Design
- 8. Staying Engaged with Low Power Cmos Design
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Low Power Cmos Design
- 9. Balancing eBooks and Physical Books Low Power Cmos Design
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Low Power Cmos Design
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Low Power Cmos Design
 - Setting Reading Goals Low Power Cmos Design
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Low Power Cmos Design
 - Fact-Checking eBook Content of Low Power Cmos Design
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development

- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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