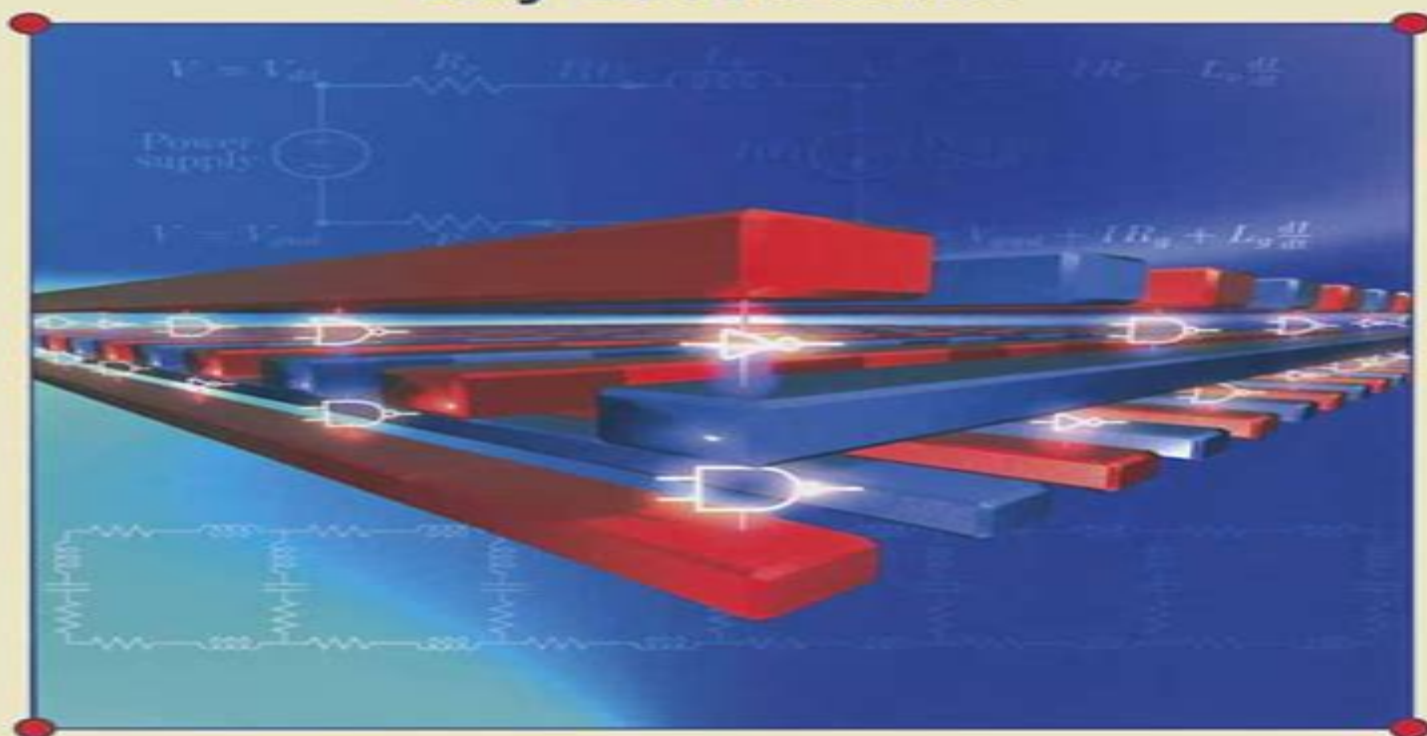


Andrey V. Mezhiba
Eby G. Friedman



Power Distribution Networks in High Speed Integrated Circuits

Kluwer Academic Publishers

Power Distribution Networks In High Speed Integrated Circuits

**Vasilis F. Pavlidis, Ioannis Savidis, Eby
G. Friedman**



Power Distribution Networks In High Speed Integrated Circuits:

Power Distribution Networks in High Speed Integrated Circuits Andrey Mezhiba, Eby G. Friedman, 2012-12-06

Distributing power in high speed high complexity integrated circuits has become a challenging task as power levels exceeding tens of watts have become commonplace while the power supply is plunging toward one volt. This book is dedicated to this important subject. The primary purpose of this monograph is to provide insight and intuition into the behavior and design of power distribution systems for high speed high complexity integrated circuits. **Power**

Distribution Networks in High Speed Integrated Circuits Andrey Mezhiba, Eby G. Friedman, 2003-11-30 *Power Distribution Networks with On-Chip Decoupling Capacitors* Mikhail Popovich, Andrey Mezhiba, Eby G. Friedman, 2007-10-08

This book provides insight into the behavior and design of power distribution systems for high speed high complexity integrated circuits. Also presented are criteria for estimating minimum required on chip decoupling capacitance. Techniques and algorithms for computer aided design of on chip power distribution networks are also described; however, the emphasis is on developing circuit intuition and understanding the principles that govern the design and operation of power distribution systems. *On-Chip Inductance in High Speed Integrated Circuits* Yehea I. Ismail, Eby G. Friedman, 2012-12-06

The appropriate interconnect model has changed several times over the past two decades due to the application of aggressive technology scaling. New more accurate interconnect models are required to manage the changing physical characteristics of integrated circuits. Currently RC models are used to analyze high resistance nets while capacitive models are used for less resistive interconnect. However, on chip inductance is becoming more important with integrated circuits operating at higher frequencies since the inductive impedance is proportional to the frequency. The operating frequencies of integrated circuits have increased dramatically over the past decade and are expected to maintain the same rate of increase over the next decade, approaching 10 GHz by the year 2012. Also, wide wires are frequently encountered in important global nets such as clock distribution networks and in upper metal layers, and performance requirements are pushing the introduction of new materials for low resistance interconnect, such as copper interconnect already used in many commercial CMOS technologies. *On-Chip Inductance in High Speed Integrated Circuits* deals with the design and analysis of integrated circuits with a specific focus on on chip inductance effects. It has been described throughout this book that inductance can have a tangible effect on current high speed integrated circuits. For example, neglecting inductance and using an RC interconnect model in a production 0.25 μm CMOS technology can cause large errors over 35% in estimates of the propagation delay of on chip interconnect. It has also been shown that including inductance in the repeater insertion design process, as compared to using an RC model, improves the overall repeater solution in terms of area, power, and delay, with average savings of 40.8%, 15.6%, and 6.7% respectively. *On-Chip Inductance in High Speed Integrated Circuits* is full of design and analysis techniques for RLC interconnect. These techniques are compared to techniques traditionally used for RC interconnect design to emphasize the

effect of inductance on Chip Inductance in High Speed Integrated Circuits will be of interest to researchers in the area of high frequency interconnect noise and high performance integrated circuit design *Power Distribution Networks with On-Chip Decoupling Capacitors* Renatas Jakushokas, Mikhail Popovich, Andrey V. Mezhiba, Selçuk Köse, Eby G. Friedman, 2010-11-23 This book describes methods for distributing power in high speed high complexity integrated circuits with power levels exceeding many tens of watts and power supplies below a volt It provides a broad and cohesive treatment of power distribution systems and related design problems including both circuit network models and design techniques for on chip decoupling capacitors providing insight and intuition into the behavior and design of on chip power distribution systems Organized into subareas to provide a more intuitive flow to the reader this second edition adds more than a hundred pages of new content including inductance models for interdigitated structures design strategies for multi layer power grids advanced methods for efficient power grid design and analysis and methodologies for simultaneously placing on chip multiple power supplies and decoupling capacitors The emphasis of this additional material is on managing the complexity of on chip power distribution networks **Three-Dimensional Integrated Circuit Design** Vasilis F. Pavlidis, Ioannis Savidis, Eby G. Friedman, 2017-07-04 Three Dimensional Integrated Circuit Design Second Edition expands the original with more than twice as much new content adding the latest developments in circuit models temperature considerations power management memory issues and heterogeneous integration 3 D IC experts Pavlidis Savidis and Friedman cover the full product development cycle throughout the book emphasizing not only physical design but also algorithms and system level considerations to increase speed while conserving energy A handy comprehensive reference or a practical design guide this book provides effective solutions to specific challenging problems concerning the design of three dimensional integrated circuits Expanded with new chapters and updates throughout based on the latest research in 3 D integration Manufacturing techniques for 3 D ICs with TSVs Electrical modeling and closed form expressions of through silicon vias Substrate noise coupling in heterogeneous 3 D ICs Design of 3 D ICs with inductive links Synchronization in 3 D ICs Variation effects on 3 D ICs Correlation of WID variations for intra tier buffers and wires Offers practical guidance on designing 3 D heterogeneous systems Provides power delivery of 3 D ICs Demonstrates the use of 3 D ICs within heterogeneous systems that include a variety of materials devices processors GPU CPU integration and more Provides experimental case studies in power delivery synchronization and thermal characterization **Power Distribution Network Design Methodologies** Istvan Novák, 2008 A series of cogently written articles by 49 industry experts this collection fills the void on Power Distribution Network PDN design procedures and addresses such related topics as DC DC converters selection of bypass capacitors DDR2 memory systems powering of FPGAs and synthesis of impedance profiles Through these contributions from such leading companies as Sun Microsystems Sanyo IBM Hewlett Packard Intel and Rambus readers will come to understand why books on power integrity are only now becoming available to the public and can relate these topics to current industry trends **On-Chip**

Power Delivery and Management Inna P. Vaisband, Renatas Jakushokas, Mikhail Popovich, Andrey V. Mezhiba, Selçuk Köse, Eby G. Friedman, 2016-04-26 This book describes methods for distributing power in high speed high complexity integrated circuits with power levels exceeding many tens of watts and power supplies below a volt It provides a broad and cohesive treatment of power delivery and management systems and related design problems including both circuit network models and design techniques for on chip decoupling capacitors providing insight and intuition into the behavior and design of on chip power distribution systems Organized into subareas to provide a more intuitive flow to the reader this fourth edition adds more than a hundred pages of new content including inductance models for interdigitated structures design strategies for multi layer power grids advanced methods for efficient power grid design and analysis and methodologies for simultaneously placing on chip multiple power supplies and decoupling capacitors The emphasis of this additional material is on managing the complexity of on chip power distribution networks *Electrical Design of Through Silicon Via* Manho Lee, Jun So Pak, Jounggho Kim, 2014-05-11 Through Silicon Via TSV is a key technology for realizing three dimensional integrated circuits 3D ICs for future high performance and low power systems with small form factors This book covers both qualitative and quantitative approaches to give insights of modeling TSV in a various viewpoints such as signal integrity power integrity and thermal integrity Most of the analysis in this book includes simulations numerical modelings and measurements for verification The author and co authors in each chapter have studied deep into TSV for many years and the accumulated technical know hows and tips for related subjects are comprehensively covered Power Distribution Network Design for VLSI Qing K. Zhu, 2004-02-19 A hands on troubleshooting guide for VLSI network designers The primary goal in VLSI very large scale integration power network design is to provide enough power lines across a chip to reduce voltage drops from the power pads to the center of the chip Voltage drops caused by the power network s metal lines coupled with transistor switching currents on the chip cause power supply noises that can affect circuit timing and performance thus providing a constant challenge for designers of high performance chips Power Distribution Network Design for VLSI provides detailed information on this critical component of circuit design and physical integration for high speed chips A vital tool for professional engineers especially those involved in the use of commercial tools as well as graduate students of engineering the text explains the design issues guidelines and CAD tools for the power distribution of the VLSI chip and package and provides numerous examples for its effective application Features of the text include An introduction to power distribution network design Design perspectives such as power network planning layout specifications decoupling capacitance insertion modeling and analysis Electromigration phenomena IR drop analysis methodology Commands and user interfaces of the VoltageStorm TM CAD tool Microprocessor design examples using on chip power distribution Flip chip and package design issues Power network measurement techniques from real silicon The author includes several case studies and a glossary of key words and basic terms to help readers understand and integrate basic concepts in VLSI design and power distribution

Multi-voltage CMOS Circuit Design

Volkan Kursun, Eby G. Friedman, 2006-08-30 This book presents an in depth treatment of various power reduction and speed enhancement techniques based on multiple supply and threshold voltages A detailed discussion of the sources of power consumption in CMOS circuits will be provided whilst focusing primarily on identifying the mechanisms by which sub threshold and gate oxide leakage currents are generated The authors present a comprehensive review of state of the art dynamic static supply and threshold voltage scaling techniques and discuss the pros and cons of supply and threshold voltage scaling techniques *Graphs in VLSI* Rassul Bairamkulov, Eby G.

Friedman, 2022-11-28 Networks are pervasive Very large scale integrated VLSI systems are no different consisting of dozens of interconnected subsystems hundreds of modules and many billions of transistors and wires Graph theory is crucial for managing and analyzing these systems In this book VLSI system design is discussed from the perspective of graph theory Starting from theoretical foundations the authors uncover the link connecting pure mathematics with practical product development This book not only provides a review of established graph theoretic practices but also discusses the latest advancements in graph theory driving modern VLSI technologies covering a wide range of design issues such as synchronization power network models and analysis and interconnect routing and synthesis Provides a practical introduction to graph theory in the context of VLSI systems engineering Reviews comprehensively graph theoretic methods and algorithms commonly used during VLSI product development process Includes a review of novel graph theoretic methods and algorithms for VLSI system design *Variation Tolerant On-Chip Interconnects* Ethiopia Enideg Nigussie, 2011-12-02

This book presents design techniques analysis and implementation of high performance and power efficient variation tolerant on chip interconnects Given the design paradigm shift to multi core interconnect centric designs and the increase in sources of variability and their impact in sub 100nm technologies this book will be an invaluable reference for anyone concerned with the design of next generation high performance electronics systems *CMOS Electronics* Jaume Segura, Charles F.

Hawkins, 2004-03-26 CMOS manufacturing environments are surrounded with symptoms that can indicate serious test design or reliability problems which in turn can affect the financial as well as the engineering bottom line This book educates readers including non engineers involved in CMOS manufacture to identify and remedy these causes This book instills the electronic knowledge that affects not just design but other important areas of manufacturing such as test reliability failure analysis yield quality issues and problems Designed specifically for the many non electronic engineers employed in the semiconductor industry who need to reliably manufacture chips at a high rate in large quantities this is a practical guide to how CMOS electronics work how failures occur and how to diagnose and avoid them Key features Builds a grasp of the basic electronics of CMOS integrated circuits and then leads the reader further to understand the mechanisms of failure Unique descriptions of circuit failure mechanisms some found previously only in research papers and others new to this publication Targeted to the CMOS industry or students headed there and not a generic introduction to the broader field of electronics

Examples exercises and problems are provided to support the self instruction of the reader *Single Flux Quantum Integrated Circuit Design* Gleb Krylov, Tahereh Jabbari, Eby G. Friedman, 2024-04-15 High efficiency large scale stationary computing systems supercomputers and data centers are becoming increasingly important due to the movement of data storage and processing onto remote cloud servers This book is dedicated to a technology particularly appropriate for this application superconductive electronics in particular rapid single flux quantum circuits The primary purpose of this book is to introduce and systematize recent developments in superconductive electronics into a cohesive whole to support the further development of large scale computing systems A brief background into the physics of superconductivity and the operation of common superconductive devices is provided followed by an introduction into different superconductive logic families including the logic gates interconnect and bias current distribution Synchronization fabrication and electronic design automation methodologies are presented reviewing both widely established concepts and techniques as well as recent approaches Issues related to memory synchronization interconnects coupling noise bias networks signal interfaces and deep scaling of superconductive structures and design for testability are described and models expressions circuits algorithms and design methodologies are discussed and placed in context The aim of this book is to provide insight and engineering intuition into the design of large scale digital superconductive circuits and systems *IEEE International Symposium on Circuits and Systems* IEEE Circuits and Systems Society, 2003 These volumes relate to matters discussed during the 2003 IEEE International Symposium on Circuits and Systems such as analogue circuits and signal processing communications multimedia systems and applications general and nonlinear circuits and systems and neural networks and systems

Man-made Catastrophes and Risk Information Concealment Dmitry Chernov, Didier Sornette, 2015-10-27 This book discusses the risks of information concealment in the context of major natural or industrial disasters offering detailed descriptions and analyses of some 25 historical cases Three Mile Island nuclear accident Bhopal disaster Challenger Space Shuttle explosion Chernobyl nuclear disaster Deepwater Horizon oil spill Fukushima Daiichi nuclear disaster Enron s bankruptcy Subprime mortgage crisis Worldwide Spanish flu and SARS outbreaks etc and applying these insights to selected on going cases where such information concealment is suspected Some successful examples of preventive anti concealment practice are also presented In the book the term concealment is used to represent the two distinct behaviors uncovered in the investigations i facts and information about an organization and its functioning being hidden from those that need them here the concealment can be due to various factors such as complexity and miscommunication to name but two and ii the conscious and deliberate action of keeping important information secret or misrepresenting it This second meaning makes up a surprisingly important part of the evidence presented Accordingly emphasis has been put on this second aspect and the approach is more pragmatic than academic remaining focused on evidence based practical and useful factors It raises awareness and provides valuable lessons for decision makers risk specialists and responsible citizens alike This work is also

intended as a fact based reference work for future academic and scholarly investigations on the roots of the problem in particular regarding any psychological or sociological modeling of human fallibility Handbook of Vibroacoustics, Noise and Harshness Naveen Garg, Chitra Gautam, Shanay Rab, Meher Wan, Ravinder Agarwal, Sanjay Yadav, 2024-12-17 The handbook covers the topics of vibro acoustics noise harshness and their related applications in detail Various topics covered in this handbook are acoustics and vibration metrology environmental noise measurements building acoustics acoustical meta materials underwater acoustics soundscape approach beam forming approach 3D noise mapping in situ acoustical testing etc The handbook would provide a single window source of up to date information to the researchers acousticians noise and vibration control engineers metrologists industry university graduates masters academicians administrators policymakers regulators and other stakeholders for a better understanding of vibro acoustics noise harshness and related applications **Advances in Machine Vision, Image Processing, and Pattern Analysis** Nanning Zheng, Xiaoyi Jiang, Xuguang Lan, 2006-08-15 This book collects the proceedings of the International Workshop on Intelligent Computing in Pattern Analysis Synthesis IWICPAS 2006 held in Xi an China alongside the 18th International Conference on Pattern Recognition ICPR 2006 The book presents 51 revised full papers and 128 revised poster papers organized in topical sections on object detection tracking and recognition pattern representation and modeling visual pattern modeling image processing compression and coding and texture analysis synthesis High-Speed Signaling Kyung Suk (Dan) Oh, Xing Chao (Chuck) Yuan, 2011-10-07 New System Level Techniques for Optimizing Signal Power Integrity in High Speed Interfaces from Pioneering Innovators at Rambus Stanford Berkeley and MIT As data communication rates accelerate well into the multi gigahertz range ensuring signal integrity both on and off chip has become crucial Signal integrity can no longer be addressed solely through improvements in package or board level design Diverse engineering teams must work together closely from the earliest design stages to identify the best system level solutions In High Speed Signaling several of the field s most respected practitioners and researchers introduce cutting edge modeling simulation and optimization techniques for meeting this challenge Edited by pioneering experts Drs Dan Oh and Chuck Yuan these contributors explain why noise and jitter are no longer separable demonstrate how to model their increasingly complex interactions and thoroughly introduce a new simulation methodology for predicting link level performance with unprecedented accuracy The authors address signal integrity from architecture through high volume production thoroughly discussing design implementation and verification Coverage includes New advances in passive channel modeling power supply noise and jitter modeling and system margin prediction Methodologies for balancing system voltage and timing budgets to improve system robustness in high volume manufacturing Practical stable formulae for converting key network parameters Improved solutions for difficult problems in the broadband modeling of interconnects Equalization techniques for optimizing channel performance Important new insights into the relationships between jitter and clocking topologies New on chip measurement techniques for in situ link

performance testing Trends and future directions in signal integrity engineering High Speed Signaling thoroughly introduces new techniques pioneered at Rambus and other leading high tech companies and universities approaches that have never before been presented with this much practical detail It will be invaluable to everyone concerned with signal integrity including signal and power integrity engineers high speed I O circuit designers and system level board design engineers

Power Distribution Networks In High Speed Integrated Circuits Book Review: Unveiling the Power of Words

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