

TRANSIENT RESPONSE OF FIRST ORDER CIRCUITS: (Chapter 8)

8.3 STEP, PULSE AND PULSE-TRAIN RESPONSES...

Pulse-Train Response of CR and RL Circuits

Figure 8.29 shows the steady-state response of the C-R and R-L circuits to a 50% duty-cycle pulse train. We observe that the current through C and the voltage across L must average to zero, for otherwise there would be unlimited energy buildup in these elements. Consequently, v_o will also average to zero, this being why the C-R and R-L circuits are also known as dc blocking circuits.

We again identify three cases of interest:

(1) $\tau \gg T$. With a long time constant there is insufficient time for appreciable energy buildup or decay in the capacitance or inductance within each subcycle. The input pulses are thus transmitted to the output with negligible distortion.

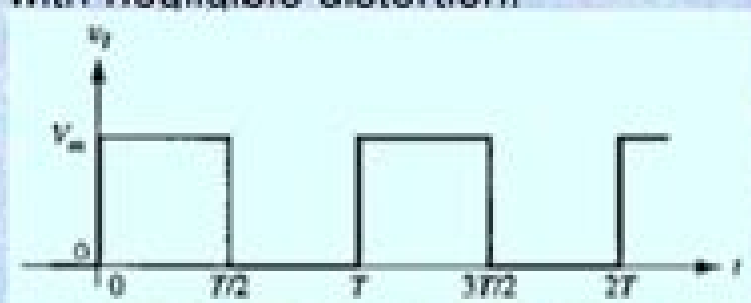


Figure 8.29(a): Input Pulse Train v_i

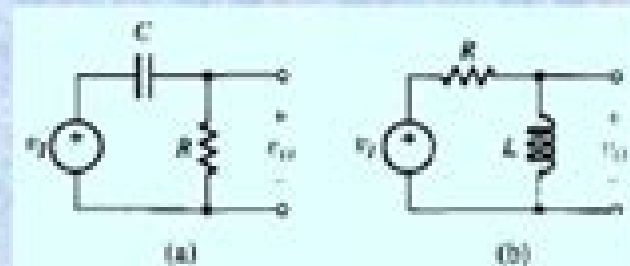


Figure 8.27 The C-R and R-L circuits.

Pulses In Communication Circuits

Tao Wei

A decorative graphic element consisting of a light blue horizontal bar with a rounded right end, and a red circular gradient shape partially visible behind it.

Pulses In Communication Circuits:

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Table of Contents Pulses In Communication Circuits

1. Understanding the eBook Pulses In Communication Circuits
 - The Rise of Digital Reading Pulses In Communication Circuits
 - Advantages of eBooks Over Traditional Books
2. Identifying Pulses In Communication Circuits
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Pulses In Communication Circuits
 - User-Friendly Interface
4. Exploring eBook Recommendations from Pulses In Communication Circuits
 - Personalized Recommendations
 - Pulses In Communication Circuits User Reviews and Ratings

- Pulses In Communication Circuits and Bestseller Lists
- 5. Accessing Pulses In Communication Circuits Free and Paid eBooks
 - Pulses In Communication Circuits Public Domain eBooks
 - Pulses In Communication Circuits eBook Subscription Services
 - Pulses In Communication Circuits Budget-Friendly Options
- 6. Navigating Pulses In Communication Circuits eBook Formats
 - ePub, PDF, MOBI, and More
 - Pulses In Communication Circuits Compatibility with Devices
 - Pulses In Communication Circuits Enhanced eBook Features
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 - Adjustable Fonts and Text Sizes of Pulses In Communication Circuits
 - Highlighting and Note-Taking Pulses In Communication Circuits
 - Interactive Elements Pulses In Communication Circuits
- 8. Staying Engaged with Pulses In Communication Circuits
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Pulses In Communication Circuits
- 9. Balancing eBooks and Physical Books Pulses In Communication Circuits
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Pulses In Communication Circuits
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Pulses In Communication Circuits
 - Setting Reading Goals Pulses In Communication Circuits
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Pulses In Communication Circuits
 - Fact-Checking eBook Content of Pulses In Communication Circuits
 - Distinguishing Credible Sources

13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
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