

Parallel Simulated Annealing Algorithm for Standard Cell Placement in VLSI Design

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ABSTRACT

Simulated Annealing (SA) is a stochastic based heuristic optimization technique based on physical process of metal crystallization. Optimization of Non-Deterministic polynomial hard (NP-hard) problems of non-trivial sizes is done using heuristic approach. Until now, simulated annealing (SA), genetic algorithm (GA) and Hopfield neural network (HNN) were individually used for solving the standard cell placement (SCP) problem. Simulated annealing established as a powerful SCP optimization tool, its drawback has always been its appetite for computational resources. In light of this, we are interested in the application of these parallel simulated annealing algorithms with respect to standard cell placement.

Several generalized algorithms proposed for parallelizing simulated annealing, only a few have been applied to cell placement. Parallel moves has been the most popular strategy and in this paper we present a new implementation of this approach.

General Terms

Standard Cell, Optimization, Parallel Moves, Non-Trivial

Keywords

NP-hard, Simulated Annealing, Hopfield Neural Network, Recombinative SA, PMSAA.

1. INTRODUCTION

The Standard Cell Placement (SCP) problem can be stated as: Give an electrical circuit consisting of fixed rectangular shaped cells and a netlist stating interconnection among terminals on the periphery of the cells and construct a layout on the periphery of the circuit itself, indicating the position of each cell such that all the nets can be routed and the total area is minimized [3].

Let $c_1, c_2, \dots, c_k$ be the cells to be placed on the chip. Each c_n , $1 \leq n \leq k$, has associated with it a height H_n and width W_n . Let $N = \{n_1, n_2, n_3, \dots, n_l\}$ be the set of nets representing the interconnections between different blocks. Let $S = \{s_1, s_2, s_3, \dots, s_k\}$ represent the empty space allocated for routing between cells. Let L_n denote the estimated length of net. The placement problem now is to determine a rectangle for each of these blocks in the row denoted by $R = \{r_1, r_2, r_3, \dots, r_k\}$ such that:

1. Each cell can be placed in the corresponding rectangle in a r_n row with width W_n and height H_n .
2. No two rectangles overlap i.e. $r_p \cap r_q = \emptyset$, $1 \leq p, q \leq k$.
3. The placement is routable, i.e. s_r , $1 \leq r \leq l$, is sufficient to route all the nets.
4. The total area of the rectangle bonding R and S is minimized, minimizing the total area of chip.
5. The total wire length is minimal.

SCP is computationally NP-hard. These problems can not be solved in polynomial time. A heuristic needs to be used to search through a large number of candidate placement configurations efficiently.

We established three heuristic techniques for SCP problem in the previous publications. They included Genetic Algorithms (GA), Hopfield Neural Network (HNN), Simulated Annealing (SA) based approach [9, 10, 11].

2. SA ALGORITHM

The Simulated Annealing Algorithm, SAA, starts with a high value of the control parameter taken for temperature; and a set of parameters $\{x_i\}$ are defined. An initial solution for a parameter x_k is computed. This initial parameter is then perturbed causing the neighbourhood parameter x_k to generate a new solution. The value of the objective function, the cost, for the new solution is computed [9, 14].

2.1 SCP by Simulated Annealing

Kirkpatrick et al. tried to solve placement and routing problems occurring in VLSI design by the SAA. A great deal of research was conducted to improve the performance of SAA for SCP [1].

Information about the initial placement of the cells on the layout is shown in the table 1 in which the first row is a sequence of cells, the second and third rows provide the coordinates of the corresponding cells on the layout.

Table 1: Representation of Standard Cell Placement

CELL	A	B	C	D	E	F	G	H	I	J
X coordinate	0	20	50	75	90	0	30	55	70	95
Y coordinate	0	0	0	0	0	50	50	50	50	50

The basic algorithm is followed by the underlined procedure.

- Initially, the starting temperature is computed, which in this case is problem-specific.
- The initial solution is generated randomly and the x and y coordinates are determined.
- To generate new solutions, the neighbourhood operator is used.

```

Read netlist (input file)
Set temperature Temp at high value
Generate an initial valid sequence of cells randomly
(Solution: Sk)
Based on the sequence K calculate x and y coordinates
of each cell
Calculate the energy Ek of the initial solution
Sbest = Sk
Ebest = Ek
LOOP
    
```

Simulated Annealing For Vlsi Design

Mikhail J. Atallah, Marina Blanton



Simulated Annealing For Vlsi Design:

Simulated Annealing for VLSI Design D.F. Wong,H.W. Leong,H.W. Liu,2012-12-06 This monograph represents a summary of our work in the last two years in applying the method of simulated annealing to the solution of problems that arise in the physical design of VLSI circuits Our study is experimental in nature in that we are concerned with issues such as solution representations neighborhood structures cost functions approximation schemes and so on in order to obtain good design results in a reasonable amount of computation time We hope that our experiences with the techniques we employed some of which indeed bear certain similarities for different problems could be useful as hints and guides for other researchers in applying the method to the solution of other problems Work reported in this monograph was partially supported by the National Science Foundation under grant MIP 87 03273 by the Semiconductor Research Corporation under contract 87 DP 109 by a grant from the General Electric Company and by a grant from the Sandia Laboratories

Simulated Annealing for VLSI Design D F Wong,H W Leong,H W Liu,1988-03-31 **Simulated Annealing** Marcos Sales Guerra Tsuzuki,2012-08-29 Simulated Annealing is a probabilistic meta heuristic that is based on statistical mechanics while at high temperatures molecules in a liquid move freely the slow reduction of temperature decreases the thermal mobility of the molecules The final state forms a pure crystal which also corresponds to a state of minimum energy We encourage readers to explore SA in their work mainly because it is simple and because it can yield very good results

Algorithms and Theory of Computation Handbook Mikhail J. Atallah,1998-11-23 Algorithms and Theory of Computation Handbook is a comprehensive collection of algorithms and data structures that also covers many theoretical issues It offers a balanced perspective that reflects the needs of practitioners including emphasis on applications within discussions on theoretical issues Chapters include information on finite precision issues as well as discussion of specific algorithms where algorithmic techniques are of special importance including graph drawing robotics forming a VLSI chip vision and image processing data compression and cryptography The book also presents some advanced topics in combinatorial optimization and parallel distributed computing applications areas where algorithms and data structuring techniques are of special importance graph drawing robot algorithms VLSI layout vision and image processing algorithms scheduling electronic cash data compression dynamic graph algorithms on line algorithms multidimensional data structures cryptography advanced topics in combinatorial optimization and parallel distributed computing Steady-State Methods for Simulating Analog and Microwave Circuits Kenneth S. Kundert,Jacob K. White,Alberto L. Sangiovanni-Vincentelli,2013-03-09 The motivation for starting the work described in this book was the interest that Hewlett Packard s microwave circuit designers had in simulation techniques that could tackle the problem of finding steady state solutions for nonlinear circuits particularly circuits containing distributed elements such as transmission lines Examining the problem of computing steady state solutions in this context has led to a collection of novel numerical algorithms which we have gathered along with some

background material into this book Although we wished to appeal to as broad an audience as possible to treat the subject in depth required maintaining a narrow focus Our compromise was to assume that the reader is familiar with basic numerical methods such as might be found in dahlquist⁷⁴ or vlach⁸³ but not assume any specialized knowledge of methods for steady state problems Although we focus on algorithms for computing steady state solutions of analog and microwave circuits the methods herein are general in nature and may find use in other disciplines A number of new algorithms are presented the contributions primarily centering around new approaches to harmonic balance and mixed frequency time methods These methods are described along with appropriate background material in what we hope is a reasonably satisfying blend of theory practice and results The theory is given so that the algorithms can be fully understood and their correctness established

A Systolic Array Optimizing Compiler Monica S. Lam, 2012-12-06 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high performance programmable systolic arrays represents a practical cost effective solution to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors

Algorithms and Theory of Computation Handbook, Volume 1 Mikhail J. Atallah, Marina Blanton, 2009-11-20 Algorithms and Theory of Computation Handbook Second Edition General Concepts and Techniques provides an up to date compendium of fundamental computer science topics and techniques It also illustrates how the topics and techniques come together to deliver efficient solutions to important practical problems Along with updating and revising many

Computational Electronics Karl Hess, J.P. Leburton, U. Ravaioli, 2013-03-14 Large computational resources are of ever increasing importance for the simulation of semiconductor processes devices and integrated circuits The Workshop on Computational Electronics was intended to be a forum for the discussion of the state of the art of device simulation Three major research areas were covered conventional simulations based on the drift diffusion and the hydrodynamic models

Monte Carlo methods and other techniques for the solution of the Boltzmann transport equation and computational approaches to quantum transport which are relevant to novel devices based on quantum interference and resonant tunneling phenomena Our goal was to bring together researchers from various disciplines that contribute to the advancement of device simulation These include Computer Science Electrical Engineering Applied Physics and Applied Mathematics The success of this multidisciplinary formula was proven by numerous interactions which took place at the Workshop and during the following three day Short Course on Computational Electronics The format of the course including a number of tutorial lectures and the large attendance of graduate students stimulated many discussions and has proven to us once more the importance of cross fertilization between the different disciplines

BiCMOS Technology and Applications Antonio R. Alvarez, 2013-03-09 The topic of bipolar compatible CMOS BiCMOS is a fascinating one and of ever growing practical importance The technology pendulum has swung from the two extremes of preeminence of bipolar in the 1950s and 60s to the apparent endless horizons for VLSI NMOS technology during the 1970s and 80s Yet starting in the 1980s several limits were clouding the horizon for pure NMOS technology CMOS reemerged as a viable high density high performance technology Similarly by the mid 1980s scaled bipolar devices had not only demonstrated new high speed records but early versions of mixed bipolar CMOS technology were being produced Hence the paradigm of either high density Q high speed was metamorphosing into an opportunity for both speed and density via a BiCMOS approach Now as we approach the 1990s there have been a number of practical demonstrations of BiCMOS both for memory and logic applications and I expect the trend to escalate over the next decade This book makes a timely contribution to the field of BiCMOS technology and circuit development The evolution is now indeed rapid so that it is difficult to make such a book exhaustive of current developments Probably equally difficult is the fact that the new technology opens a range of novel circuit opportunities that are as yet only formative in their development Given these obstacles it is a herculean task to try to assemble a book on BiCMOS

Mixed-Mode Simulation Resve A. Saleh, A. Richard Newton, 2012-12-06 Our purpose in writing this book was two fold First we wanted to compile a chronology of the research in the field of mixed mode simulation over the last ten to fifteen years A substantial amount of work was done during this period of time but most of it was published in archival form in Masters theses and Ph D dissertations Since the interest in mixed mode simulation is growing and a thorough review of the state of the art in the area was not readily available we thought it appropriate to publish the information in the form of a book Secondly we wanted to provide enough information to the reader so that a proto type mixed mode simulator could be developed using the algorithms in this book The SPLICE family of programs is based on the algorithms and techniques described in this book and so it can also serve as documentation for these programs

ACKNOWLEDGEMENTS The authors would like to dedicate this book to Prof D O Peder son for inspiring this research work and for providing many years of support and encouragement The authors enjoyed many fruitful discussions and collaborations with Jim Kleckner Young Kim

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