

Coupled device, circuit and interconnect simulation

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Abstract:

In this paper, we discuss several aspects that are related to coupling device, circuit and interconnect simulation software. Straightforward co-simulation is too time-consuming, and hence reduced order modelling must be used in order to summarize the behaviour of individual simulations into compact models. From a theoretical point of view, the problem is complicated by the fact that equations of different type are being coupled. Mathematical techniques are indispensable for guaranteeing acceptable simulation times.

The European project CODESTAR aims at providing a framework in which the aforementioned coupled simulations can be performed. The examples given in this paper have been taken from that project.

1. Introduction

For the design of complex integrated systems, knowledge of the electromagnetic coupling in passive components like inductors, capacitors and critical parts of net lists are indispensable. Today's extraction software tools use the static approach to quantify this coupling, thereby ignoring the Maxwell or wave-dynamic aspect of electromagnetic radiation. Whereas such an approach is valid at moderate frequencies, high-frequency effects are a major design concern for the next generation of architectures. The International Technology Roadmap for Semiconductors recognizes the lack of appropriate future design tools. In particular design tools that include high frequency effects are a difficult challenge for a successful implementation of the 65 nm node corresponding to circuit frequencies exceeding 5 GHz. The effects are physically understood, but TCAD software programs that can deal with them are not available. Figure 1 (inspired by [6]) summarizes the effects that play a role in the analysis of passive structures: electric and magnetic coupling of segments through air and oxide, current crowding at edges due to the skin effect and eddy currents, proximity effects due to presence of nearby segments, radiation, substrate injection, and substrate current caused by ohmic, eddy and displacement currents.

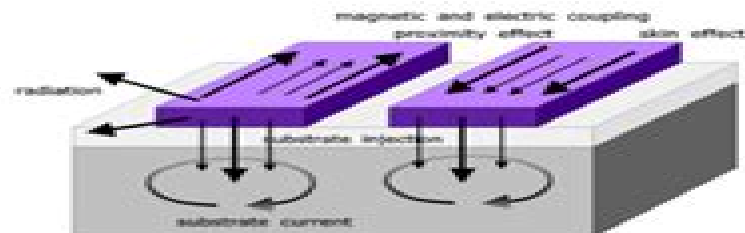


Figure 1. Summary of effects occurring in passive structures.

To accelerate the design of high-frequency passive on-chip structures and interconnects, the development of new modelling algorithms is needed. This task is addressed in the CODESTAR project. The resulting software will be used in a design cycle, starting from standardized geometrical data (GDS II format), and returning as output a manageable simulation net list that can be coupled to a network simulator such as SPICE or Pstar.

The situation becomes even more complicated when substrate noise analysis is required. As feature sizes decrease, substrate coupling noise may cause design failures and poor yields due to injected currents disturbing the operation of sensitive components. Any design targeted at sub-quarter micron process technologies may be vulnerable to substrate parasitics. Rule of thumb methodologies may turn out to be inadequate or lead to over-engineered designs. Reliable results can only be obtained by taking into account semiconductor physics. Tools like SubstrateStorm from Cadence perform such analyses by supplying RC net lists and reduced RC net lists, which can be coupled to network simulators. More accurate results are obtained when drift-diffusion models of semiconductor devices are used. In section 3 an example is given discussing precisely this topic, showing that it is indeed possible to couple device, circuit and interconnect simulations to obtain reliable models for substrate coupling noise.

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