Reconfigurable Processor Array A Bit Sliced Parallel Computer (USA)

Rushton, A.

Reconfigurable Processor Array A Bit Sliced Parallel Computer Usa Paperback

Maya B. Gokhale,Brian Schott,Institute for Defense Analyses

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Principles of Auditing/Study Guide Walter B. Meigs,E. Larsen,R. Meigs,1988-12-01 **Reconfigurable Processor Array A Bit Sliced Parallel Computer (Usa)** A. Rushton,Efraim Turban,Jack R. Meredith,1991-08 **Reconfigurable Processor-array** Andrew Rushton,1989-01-01 **Forthcoming Books** Rose Arny,1989-05 **Publishers Trade List Annual, 1992** ,1992 *Paperbound Books in Print* ,1991 **The Publishers' Trade List Annual** ,1992 *Whitaker's Book List* ,1989 *The British National Bibliography* Arthur James Wells,1968 *Whitaker's Books in Print* ,1998 **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1987 Issues for 1973 cover the entire IEEE technical literature **Science Abstracts** ,1993 Reconfigurable Massively Parallel Computers Hungwen Li,Quentin F. Stout,1991 Offers guidance on three areas of the complex world of reconfigurable massively parallel computers architecture mapping algorithms to the architecture and fault tolerance The material is addressed to students and professionals interested in the exploitation of array processing Data Parallel C on a Reconfigurable Logic Array Maya B. Gokhale,Brian Schott,Institute for Defense Analyses,1994 Abstract The existence of reconfigurable logic arrays has made it possible to create on the same physical hardware platform many different virtual circuits a configuration bit stream loaded into the logic array determines the virtual circuit which is to be emulated The virtual logic can be used to create new instructions which supplement the instruction set of a conventional processor as demonstrated for example in 2 and 3 or alternatively can operate as a parallel co processor as shown in the Splash systems 8 and 9 The ease of hardware reconfiguration has not been accompanied by a corresponding capability in the software environment In most cases schematic capture tools textual hardware description languages or low level vendor specific tools must be used to create new configurations Research into high level synthesis for reconfigurable arrays has begun however as evidenced by the PRISM 2 tools of 3 and the dbC translation system of 9 The ability to write algorithms for these arrays in high level procedural language is key to their effective use In this paper we describe the data parallel bit C system which is used to program a reconfigurable logic array as a custom SIMD co processor The dbC language has bit oriented extensions to C which give the programmer control over the size of parallel data objects so that the data size requirements of the algorithm can be accurately reflected in the hardware The data parallel extensions provide the ability to define a SIMD processor array to operate on data in the processors memories to perform global reductions over the processor array and to communicate data between nearest neighbor processing elements We describe the major components of our translation system and show how it is mapped onto the Splash 2 system **Reconfigurable Processor Array** A. Rushton,E Jerome McCarthy,1991-02 **Reconfigurable Computer Array** ,1998 A universal limitation of RF and imaging front end sensors is that they easily produce data at a higher rate than any general purpose computer can continuously handle Therefore Los Alamos National Laboratory has developed a custom Reconfigurable Computing Array board to support a large variety of processing

applications including wideband RF signals LIDAR and multi dimensional imaging The boards design exploits three key features to achieve its performance First there are large banks of fast memory dedicated to each reconfigurable processor and also shared between pairs of processors Second there are dedicated data paths between processors and from a processor to flexible I O interfaces Third the design provides the ability to link multiple boards into a serial and or parallel structure   *Augmenting a Microprocessor with Reconfigurable Hardware* John Reid Hauser,2000   **Design of a Bit-sliced Processor Array with Built-in-self-test** Paul Chunhei Mui,1984 The overall objective of this report is to present an integrated approach to the design of bit sliced processor arrays with built in self test The conventional approach of making each bit sliced processor chip self testing is not used Rather a new approach of using an extra chip to test a processor array fo any size and itself is used The classical stuck at fault model is not suitable for VLSI circuits Rather a functional level fault model is used Ech module of the processor array is tested exhaustively The test responses of a fault free processor array are made identical so that they can be easily monitored with no loss in fault coverage The tester chip tests itself while it is testing the processor array The fault coverages for both the tester chip and the processor array are high the performance degradation is minimal the area overhead is low especially for large processor arrays and the test length is short so tests can be performed more frequently A VLSI design of the tester chip has been done with a 2 microns NMOS process Author   LUCAS Associative Array Processor Christer Fernstrom,Ivan Kruzela,Bertil Svensson,1986   **A Computer Architecture Based on Reconfigurable Co-processor Modules** Mehmet Can Ertem,1986

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