

Reconfigurable Processor Array

A Bit Sliced Parallel Computer

(USA)

Reconfigurable Processor Array A Bit Sliced Parallel Computer

Michael Rajnik



Reconfigurable Processor Array A Bit Sliced Parallel Computer:

Reconfigurable Processor Array A Bit Sliced Parallel Computer (Usa) A. Rushton,1991-02 *Reconfigurable Processor-array* Andrew Rushton,1989 This book investigates enhancements to the conventional bit serial PE with the aim of improving its performance in situations where the small grain parallelism of a single instruction stream multiple data stream SIMD class parallel computer architecture is inefficient Principles of Auditing/Study Guide Walter B. Meigs,E. Larsen,R. Meigs,1988-12-01 *Occam and the Transputers, Current Developments* World Occam and Transputer User Group. Technical Meeting,1991 Examines applications of transputers and OCCAM including numerical image processing neural networks natural language processing networks and biological systems as well as tools routeing and mapping The T9000 new generation transputer introduction is further discussed **Massively Parallel Computing with the DAP** Dennis Parkinson,John Litt,1990 This monograph outlines the development of the DAP Distributed Array of Processors system which provides massively parallel fine grain processing The selection of papers covers the history programming and some of the applications of the DAP Parallel Database Processing Peter Willett,Edie M. Rasmussen,1990 Execution Models of Prolog for Parallel Computers Péter Kacsuk,1990 The research described in this book addresses the semantic gap between logic programming languages and the architecture of parallel computers the problem of how to implement logic programming languages on parallel computers in a way that can most effectively exploit the inherent parallelism of the language and efficiently utilize the parallel architecture of the computer Following a useful review of other research results the first project explores the possibilities of implementing logic programs on MIMD nonshared memory massively parallel computers containing 100 to 1 000 processing elements The second investigates the possibility of implementing Prolog on a typical SIMD machine called a Distributed Processor Array The author s objectives are to define a parallel computational paradigm the Extended Cellular Dataflow Model that can be used to create a Parallel Prolog Abstract Machine as a general starting point for implementing logic programming languages on parallel computers to exploit the different types of parallelism of these programs to define an efficient parallel logic machine to explore the possibilities of implementing logic programming languages on array processors such as the DAP to invent parallel implementation techniques for effectively executing Prolog on the DAP and to define a parallel extension of Prolog that is able to utilize the processor aggregate of the DAP for effectively solving numerical subproblems within logic programs Peter Kacsuk is with Multilogic Computing Ltd of Budapest Hungary **Computer Architecture** Robert J. Baron,Lee Higbie,1992 Computer Architecture offers an overview of a computer s key structural building blocks introducing these building blocks in terms of computer family architecture whose members maintain compatibility with prior generation hardware as new implementations are introduced *Languages and Compilers for Parallel Computing* David Hillel Gelernter,Alexandru Nicolau,David A. Padua,1990 A collection of papers examining the languages and compilers for parallel computing It covers a wide variety of topics ranging

from improving parallel program performance using critical path analysis to software engineering of parallel programs in the computation orientated display environment **Languages and Compilers for Parallel Computing** David Gelernter, Alexandru Nicolau, David A. Padua, 1990 A collection of papers examining the languages and compilers for parallel computing It covers a wide variety of topics ranging from improving parallel program performance using critical path analysis to software engineering of parallel programs in the computation orientated display environment **Parallel SML** Kevin Hammond, 1991 **Computers and Artificial Intelligence**, 1991 **Advances in Languages and Compilers for Parallel Processing** Alexandru Nicolau, 1991 Mathematics of Computing Parallelism **Implementation of a General-purpose Dataflow Multiprocessor** Gregory Michael Papadopoulos, 1991 *Partitioning and Scheduling Parallel Programs for Multiprocessors* Vivek Sarkar, 1989 This book is one of the first to address the problem of forming useful parallelism from potential parallelism and to provide a general solution The book presents two approaches to automatic partitioning and scheduling so that the same parallel program can be made to execute efficiently on widely different multiprocessors The first approach is based on a macro dataflow model in which the program is partitioned into tasks at compile time and the tasks are scheduled on processors at run time The second approach is based on a compile time scheduling model where both the partitioning and scheduling are performed at compile time Both approaches have been implemented in partition programs written in the single assignment language SISAL The inputs to the partitioning and scheduling algorithms are a graphical representation of the parallel program and a list of parameters describing the target multiprocessor Execution profile information is used to derive compile time estimates of execution times and data sizes in the program Both the macro dataflow and compile time scheduling problems are expressed as optimization problems and are shown to be NP complete in the strong sense Efficient approximation algorithms for these problems are presented Finally the effectiveness of the partitioning and scheduling algorithms is studied by multiprocessor simulations of various SISAL benchmark programs for different target multiprocessor parameters Vivek Sarkar is a Member of Research Staff at the IBM T J Watson Research Center Partitioning and Scheduling Parallel Programs for Multiprocessing is included in the series Research Monographs in Parallel and Distributed Computing Copublished with Pitman Publishing New Technical Books New York Public Library, 1991 Languages and Compilers for Parallel Computing Lawrence Rauchwerger, 2019-11-19 This book constitutes the proceedings of the 30th International Workshop on Languages and Compilers for Parallel Computing LCPC 2017 held in College Station TX USA in October 2017 The 17 full papers presented together with abstracts of 5 keynote talks 11 invited speakers and 4 poster papers in this volume were carefully reviewed and selected from 26 submissions LCPC encourages submissions that go outside its original scope of scientific computing to diverse areas that are enable or enhanced by the power of parallel systems such as mobile computing big data relevant aspects of machine learning data centers cognitive computing etc LCPC strongly encourages personal interaction and technical discussions along the

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