

Multilevel-Spiral Inductors Using VLSI Interconnect Technology

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Abstract—A multilevel-spiral (MLS) inductor structure for implementation in VLSI interconnect technology is presented. Inductances of 8.8 and 32 nH and maximum quality-factors (Q) of ~ 6.8 and 3.6, respectively, are achieved in a four-level metal BiCMOS technology, with four turns at each of the two or four stacked spiral coils and with an area of $126 \times 126 \mu\text{m}^2$. The comparison of the MLS inductors to different single-level-spiral (SLS) control devices shows that a MLS inductor provides the same inductance at $\sim 50\%$ dc resistance, but the maximum Q is typically measured at a lower frequency and the self-resonance frequency is reduced due to a high inter-wire capacitance.

I. INTRODUCTION

THE INTEGRATION of inductors on a silicon substrate presents a difficult task due to the substrate losses and the limited thickness of the VLSI interconnects [1], [2]. Adequate inductance (L) and quality-factors (Q) have mostly been achieved through considerable deviations from standard silicon processing [3]–[5], but recent developments have shown that conventional multilevel interconnects can be utilized to match or surpass the best results in the frequency range from 900 MHz to 2.4 GHz [6]. Multilevel interconnects can be exploited for inductor integration in three different ways: 1) several metal layers can be shunted in parallel to achieve an effective conductor thickness beyond the metal thickness limit [6], [7]; 2) the lower metal levels can be excluded to increase the spacing between inductor and substrate and thus reduce substrate losses [6]; and 3) the spiral coil can be extended over several interconnect levels in order to assimilate a solenoidal inductor, i.e., a multilevel-spiral (MLS) inductor structure, for an increased inductance/area value [8].

In this paper, we present a new MLS inductor structure in which no underpasses to the center contact or between the turns are used, so that a given inductance is achieved at minimum wire length and thus minimum resistance. Further, we discuss the design trade-offs for the MLS structure and make for the first time a detailed experimental comparison to the single-level-spiral (SLS) structure, which is important for establishing the optimum application of either structure.

II. INDUCTOR STRUCTURES AND FABRICATION

Fig. 1 shows the plan views of a SLS inductor on a silicon substrate (Fig. 1(a)), as originally proposed by Nguyen and Meyer [1], and two configurations of the new MLS

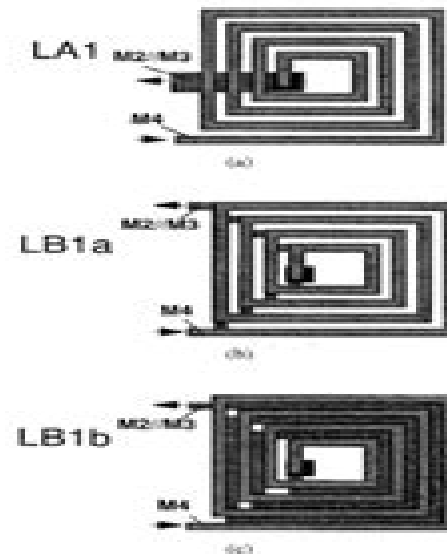


Fig. 1. Schematic plan views of a conventional single-level-spiral inductor with (a) a straight underpass contact (LA1), and of two configurations of the new multilevel-spiral inductor structure (LB1a and (c)), LB1b). The two-level-spiral structures differ in that the lower spiral was placed either in the spaces of the upper coil ((c), LB1b) or with a maximum overlap ((b), LB1a). The upper coil was fabricated by using the metal layer M4 while the straight underpass in LA1 and the lower coils in LB1a and LB1b used shunted M2 and M3 levels (M2/M3).

structure (Fig. 1(b) and (c)). The spiral coil of the SLS device can be built with one metal layer [1], [2] or with several shunted metal layers in parallel [6], [7], but in any of those structures, an additional metal level is required to form a straight underpass contact which itself adds very little inductance. The basic idea of the new MLS structures was to replace the straight underpass by a second spiral coil to generate additional magnetic flux and arrive at a higher inductance value for the same inductor area and metal pitch. The concept uses an upper coil which spirals in to a center contact to a lower coil which spirals out in the same sense. Magnetic flux is therefore generated at minimum wire length

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 - Advantages of eBooks Over Traditional Books
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 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Multilevel Interconnect Technology Ii Spie Proceedings Series
 - User-Friendly Interface
4. Exploring eBook Recommendations from Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Personalized Recommendations
 - Multilevel Interconnect Technology Ii Spie Proceedings Series User Reviews and Ratings
 - Multilevel Interconnect Technology Ii Spie Proceedings Series and Bestseller Lists
5. Accessing Multilevel Interconnect Technology Ii Spie Proceedings Series Free and Paid eBooks
 - Multilevel Interconnect Technology Ii Spie Proceedings Series Public Domain eBooks
 - Multilevel Interconnect Technology Ii Spie Proceedings Series eBook Subscription Services
 - Multilevel Interconnect Technology Ii Spie Proceedings Series Budget-Friendly Options
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- Multilevel Interconnect Technology Ii Spie Proceedings Series Compatibility with Devices
- Multilevel Interconnect Technology Ii Spie Proceedings Series Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Highlighting and Note-Taking Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Interactive Elements Multilevel Interconnect Technology Ii Spie Proceedings Series
- 8. Staying Engaged with Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Multilevel Interconnect Technology Ii Spie Proceedings Series
- 9. Balancing eBooks and Physical Books Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Multilevel Interconnect Technology Ii Spie Proceedings Series
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Setting Reading Goals Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Fact-Checking eBook Content of Multilevel Interconnect Technology Ii Spie Proceedings Series
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
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 - Interactive and Gamified eBooks

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