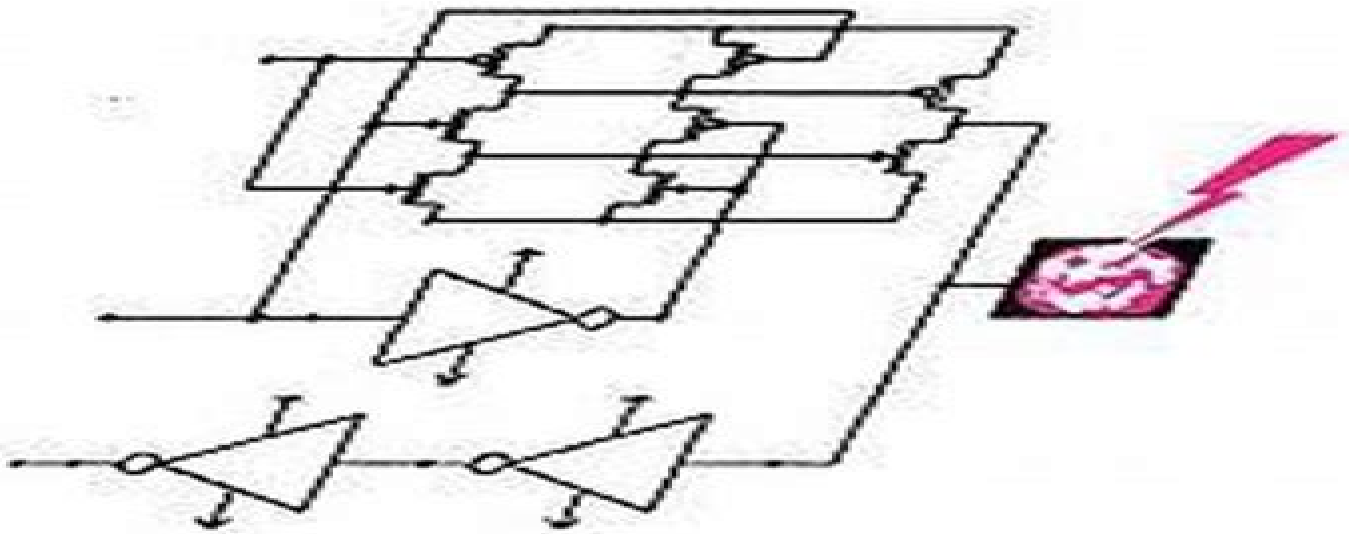
MODELING OF ELECTRICAL OVERSTRESS IN INTEGRATED CIRCUITS



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Modeling Of Electrical Overstress In Integrated Circuits

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Modeling Of Electrical Overstress In Integrated Circuits:

Modeling of Electrical Overstress in Integrated Circuits Carlos H. Diaz,Sung-Mo (Steve) Kang,Charvaka Duvvury,2012-12-06 Electrical overstress EOS and Electrostatic discharge ESD pose one of the most dominant threats to integrated circuits ICs These reliability concerns are becoming more serious with the downward scaling of device feature sizes Modeling of Electrical Overstress in Integrated Circuits presents a comprehensive analysis of EOS ESD related failures in I O protection devices in integrated circuits The design of I O protection circuits has been done in a hit or miss way due to the lack of systematic analysis tools and concrete design guidelines In general the development of on chip protection structures is a lengthy expensive iterative process that involves tester design fabrication testing and redesign When the technology is changed the same process has to be repeated almost entirely This can be attributed to the lack of efficient CAD tools capable of simulating the device behavior up to the onset of failure which is a 3 D electrothermal problem For these reasons it is important to develop and use an adequate measure of the EOS robustness of integrated circuits in order to address the on chip EOS protection issue Fundamental understanding of the physical phenomena leading to device failures under ESD EOS events is needed for the development of device models and CAD tools that can efficiently describe the device behavior up to the onset of thermal failure Modeling of Electrical Overstress in Integrated Circuits is for VLSI designers and reliability engineers particularly those who are working on the development of EOS ESD analysis tools CAD engineers working on development of circuit level and device level electrothermal simulators will also benefit from the material covered This book will also be of interest to researchers and first and second year graduate students working in semiconductor devices and IC reliability fields **Modeling and Simulation of Electrical Overstress Failures in Input/output Protection Devices of Integrated Circuits** Carlos Hernando Diaz,1993 It is proposed in this thesis that a measure to determine the electrical overstress EOS hardness of integrated circuits with respect to EOS electrostatic discharge ESD can be measured in terms of the power vs time to failure relationship power profile and the current vs time to failure relationship current profile A new nonlinear mixed 2D 1D thermal simulator iTSIM was developed in order to understand and quantify the sensitivity of the power profiles with respect to major thermal parameters of the integrated circuit IC Protection devices with different layout parameters were fabricated and experimentally characterized for EOS Experimental data indicate that these devices fail with a poly gate filament in the drain edge when subjected to ESD or short duration EOS events while extensive device damage is observed for long duration EOS events revealing onset of thermal runaway Two dimensional 2D device level electrothermal simulations are used to develop qualitative analysis of both the physical mechanisms leading to device failure and the dependencies of the failure thresholds power and current profiles on the layout parameters Results from this study coupled with heat removal considerations led to a design guideline for source contact placement that is expected to improve the failure thresholds for I O protection devices of CMOS ICs with grounded substrate Thermal instability of an

electrically stressed circuit or device is shown to be the result of either thermally induced negative differential resistance NDR in resistive regions or junction second breakdown Under typical ESD EOS stress events transient in nature the temperature at which thermal instability takes place depends on the level of the stress current In semiconductor junctions reverse biased by an EOS event second breakdown is shown to happen at the time when thermal carrier generation becomes high enough to offset the effects of the mobility degradation and the reduction of the impact ionization rates Under these circumstances the time for the onset of second breakdown is shown to depend on the device s geometry and the level of power dissipation Circuit level electrothermal models are introduced for resistors diodes and bipolar and MOS transistors they are capable of describing device behaviour up into thermal runaway or second breakdown Abstract shortened by UMI

On-Chip ESD Protection for Integrated Circuits Albert Z.H. Wang,2006-01-03 This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer s perspective On Chip ESD Protection for Integrated Circuits An IC Design Perspective provides both fundamental and advanced materials needed by a circuit designer for designing ESD protection circuits including Testing models and standards adopted by U S Department of Defense EIA JEDEC ESD Association Automotive Electronics Council International Electrotechnical Commission etc ESD failure analysis protection devices and protection of sub circuits Whole chip ESD protection and ESD to circuit interactions Advanced low parasitic compact ESD protection structures for RF and mixed signal IC s Mixed mode ESD simulation design methodologies for design prediction ESD to circuit interactions and more Many real world ESD protection circuit design examples are provided The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field Electrical Overstress (EOS) Steven H. Voldman,2013-10-28 Electrical Overstress EOS continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures The text provides a clear picture of EOS phenomena EOS origins EOS sources EOS physics EOS failure mechanisms and EOS on chip and system design It provides an illuminating insight into the sources of EOS in manufacturing integration of on chip and system level EOS protection networks followed by examples in specific technologies circuits and chips The book is unique in covering the EOS manufacturing issues from on chip design and electronic design automation to factory level EOS program management in today s modern world Look inside for extensive coverage on Fundamentals of electrical overstress from EOS physics EOS time scales safe operating area SOA to physical models for EOS phenomena EOS sources in today s semiconductor manufacturing environment and EOS program management handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices circuits and system Discussion of how to distinguish between EOS events and electrostatic discharge ESD events e g such as human body model HBM charged device model CDM cable discharge events CDM charged board events CBE to system level IEC 61000 4 2 test events EOS protection on chip design

practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards PCB and manufacturing equipment Examples of EOS issues in state of the art digital analog and power technologies including CMOS LDMOS and BCD EOS design rule checking DRC LVS and ERC electronic design automation EDA and how it is distinct from ESD EDA systems EOS testing and qualification techniques and Practical off chip ESD protection and system level solutions to provide more robust systems Electrical Overstress EOS Devices Circuits and Systems is a continuation of the author s series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano electronic era *Simulation Methods for ESD Protection Development* Harald Gossner,Kai Esmark,Wolfgang Stadler,2003-10-16 Simulation Methods for ESD Protection Development looks at the integration of new techniques into a comprehensive development flow which is now available due advances made in the field during the recent years These findings allow for an early stable ESD concept at a very early stage of the technology development which is essential now development cycles have been reduced The book also offers ways of increasing the optimization and control of the technology concerning performance thus making the process more cost effective and increasingly efficient This title provides a guide through the latest research and technology presenting the ESD protection development methodology This is based on a combination of process device and circuit stimulation and addresses the optimization of the industry critical issue reduced development cycles Written to address the needs of the ESD engineer this text is required reading by all industry practitioners and researchers and students within this field The FIRST Extensive overview on the subject of ESD simulation Addresses the industry critical issue of reduced development cycles and provides solutions Presents the latest research in the field with high practical relevance and its results *Integrated Circuit Test Engineering* Ian A. Grout,2005-12-08 Taking a three pronged approach test engineering from traditional test design and manufacturing view points Integrated Circuit Test Engineering encapsulates the subject as it stands today After introductory background from basic testing rules to trends in technology the reader learns about fabrication processes a complete range of detailed tests and procedures how to design for testability fault simulation automatic test equipment and the economics of testing The text incudes Worked examples and exercises well organized references and bibliography An introduction to the use of various software and languages such as MATLAB Spice Verilog HDL and VHDL A series of experiments based on material downloaded from springeronline com showing how to construct a hardware test arrangement for MS Windows PCs This book is a practical tool for advanced undergraduate and graduate electronic engineering students a resource for their tutors and a guide for the practising electronic engineer Electrothermal Analysis of VLSI Systems Yi-Kan Cheng,Ching-Han Tsai,Chin-Chi Teng,Sung-Mo (Steve) Kang,2005-12-01 This useful book addresses electrothermal problems in modern VLSI systems It discusses electrothermal phenomena and the fundamental building blocks that electrothermal simulation requires The authors present three important applications of VLSI electrothermal analysis temperature dependent

electromigration diagnosis cell level thermal placement and temperature driven power and timing analysis *ESD Testing* Steven H. Voldman,2016-10-07 With the evolution of semiconductor technology and global diversification of the semiconductor business testing of semiconductor devices to systems for electrostatic discharge ESD and electrical overstress EOS has increased in importance ESD Testing From Components to Systems updates the reader in the new tests test models and techniques in the characterization of semiconductor components for ESD EOS and latchup Key features Provides understanding and knowledge of ESD models and specifications including human body model HBM machine model MM charged device model CDM charged board model CBM cable discharge events CDE human metal model HMM IEC 61000 4 2 and IEC 61000 4 5 Discusses new testing methodologies such as transmission line pulse TLP to very fast transmission line pulse VF TLP and future methods of long pulse TLP to ultra fast TLP UF TLP Describes both conventional testing and new testing techniques for both chip and system level evaluation Addresses EOS testing electromagnetic compatibility EMC scanning to current reconstruction methods Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing ESD Testing From Components to Systems is part of the authors series of books on electrostatic discharge ESD protection this book will be an invaluable reference for the professional semiconductor chip and system level ESD and EOS test engineer Semiconductor device and process development circuit designers quality reliability and failure analysis engineers will also find it an essential reference In addition its academic treatment will appeal to both senior and graduate students with interests in semiconductor process device physics semiconductor testing and experimental work **Field-Programmable Analog Arrays** Edmund Pierzchala,Glenn Gulak,Leon Chua,Angel Rodríguez-Vázquez,2013-06-29 Field Programmable Analog Arrays brings together in one place important contributions and up to date research results in this fast moving area Field Programmable Analog Arrays serves as an excellent reference providing insight into some of the most challenging research issues in the field Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Nadine Azemard,Lars Svensson,2007-08-21 This volume features the refereed proceedings of the 17th International Workshop on Power and Timing Modeling Optimization and Simulation Papers cover high level design low power design techniques low power analog circuits statistical static timing analysis power modeling and optimization low power routing optimization security and asynchronous design low power applications modeling and optimization and more Reliability Modeling: The RIAC Guide to Reliability Prediction, Assessment and Estimation William Denson,2006 The intent of this book is to provide guidance on modeling techniques that can be used to quantify the reliability of a product or system In this context reliability modeling is the process of constructing a mathematical model that is used to estimate the reliability characteristics of a product There are many ways in which this can be accomplished depending on the product or system and the type of information that is available or practical to obtain This book reviews possible approaches summarizes their advantages and disadvantages and provides guidance on selecting a

methodology based on the specific goals and constraints of the analyst While this book will not discuss the use of specific published methodologies in cases where examples are provided tools and methodologies with which the author has personal experience in their development are used such as life modeling NPRD MIL HDBK 217 and the RIAC 217Plus Introduction

Transient-Induced Latchup in CMOS Integrated Circuits Ming-Dou Ker,Sheng-Fu Hsu,2009-07-23 The book all semiconductor device engineers must read to gain a practical feel for latchup induced failure to produce lower cost and higher density chips Transient Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup explaining the critical issues that have resurfaced for CMOS technologies Once readers can gain an understanding of the standard practices for TLU Ker and Hsu discuss the physical mechanism of TLU under a system level ESD test while introducing an efficient component level TLU measurement setup The authors then present experimental methodologies to extract safe and area efficient compact layout rules for latchup prevention including layout rules for I O cells internal circuits and between I O and internal circuits The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0 18 micrometer 1 8V 3 3V silicided CMOS process Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time to market Written by experts with real world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system level ESD and EFT tests This book is essential for practicing engineers involved in IC design IC design management system and application design reliability and failure analysis Undergraduate and postgraduate students specializing in CMOS circuit design and layout will find this book to be a valuable introduction to real world industry problems and a key reference during the course of their careers *The ESD Handbook* Steven H. Voldman,2021-04-12 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific

and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems Parasitic Substrate Coupling in High Voltage Integrated Circuits Pietro Buccella,Camillo Stefanucci,Maher Kayal,Jean-Michel Sallese,2018-03-14 This book introduces a new approach to model and predict substrate parasitic failures in integrated circuits with standard circuit design tools The injection of majority and minority carriers in the substrate is a recurring problem in smart power ICs containing high voltage high current switching devices besides sensitive control protection and signal processing circuits The injection of parasitic charges leads to the activation of substrate bipolar transistors This book explores how these events can be evaluated for a wide range of circuit topologies To this purpose new generalized devices implemented in Verilog A are used to model the substrate with standard circuit simulators This approach was able to predict for the first time the activation of a latch up in real circuits through post layout SPICE simulation analysis Discusses substrate modeling and circuit level simulation of parasitic bipolar device coupling effects in integrated circuits Includes circuit back annotation of the parasitic lateral n p n and vertical p n p bipolar transistors in the substrate Uses Spice for simulation and characterization of parasitic bipolar transistors latch up of the parasitic p n p n structure and electrostatic discharge ESD protection devices Offers design guidelines to reduce couplings by adding specific protections **ESD** Steven H. Voldman,2011-04-04 Electrostatic discharge ESD continues to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a whole chip ESD design synthesis approach It provides a clear insight into the integration of ESD protection networks from a generalist perspective followed by examples in specific technologies circuits and chips Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a top down design approach Look inside for extensive coverage on integration of cores power bussing and signal pins in DRAM SRAM CMOS image processing chips microprocessors analog products RF components and how the integration influences ESD design and integration architecturing of mixed voltage mixed signal to RF design for ESD analysis floorplanning for peripheral and core I O designs and the implications on ESD and latchup guard ring integration for both a bottom up and top down methodology addressing I O guard rings ESD guard rings I O to I O and I O to core classification of ESD power clamps and ESD signal pin circuitry and how to make the correct choice for a given semiconductor chip examples of ESD design for the state of the art technologies discussed including CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVCMOS RF CMOS and smart power practical methods for the understanding of ESD circuit power distribution ground rule development internal bus distribution current path analysis quality metrics ESD Design and Synthesis is a continuation of the author s series of books on ESD protection It is an essential reference for ESD circuit and semiconductor engineers design synthesis team leaders

layout design characterisation floorplanning test and reliability engineers technicians and groundrule and test site developers in the manufacturing and design of semiconductor chips It is also useful for graduate and undergraduate students in electrical engineering semiconductor sciences and manufacturing sciences and on courses involving the design of ESD devices chips and systems This book offers a useful insight into the issues that confront modern technology as we enter the nano electronic era *Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits* Nishath K. Verghese,Timothy J. Schmerbeck,David J. Allstot,2012-12-06 The goal of putting systems on a chip has been a difficult challenge that is only recently being met Since the world is analog putting systems on a chip requires putting analog interfaces on the same chip as digital processing functions Since some processing functions are accomplished more efficiently in analog circuitry chips with a large amount of analog and digital circuitry are being designed Whether a small amount of analog circuitry is combined with varying amounts of digital circuitry or the other way around the problem encountered in marrying analog and digital circuitry are the same but with different scope Some of the most prevalent problems are chip package capacitive and inductive coupling ringing on the RLC tuned circuits that form the chip package power supply rails and off chip drivers and receivers coupling between circuits through the chip substrate bulk and radiated emissions from the chip package interconnects To aggravate the problems of designers who have to deal with the complexity of mixed signal coupling there is a lack of verification techniques to simulate the problem In addition to considering RLC models for the various chip package board level parasitics mixed signal circuit designers must also model coupling through the common substrate when simulating ICs to obtain an accurate estimate of coupled noise in their designs Unfortunately accurate simulation of substrate coupling has only recently begun to receive attention and techniques for the same are not widely known Simulation Techniques and Solutions for Mixed Signal Coupling in Integrated Circuits addresses two major issues of the mixed signal coupling problem how to simulate it and how to overcome it It identifies some of the problems that will be encountered gives examples of actual hardware experiences offers simulation techniques and suggests possible solutions Readers of this book should come away with a clear directive to simulate their design for interactions prior to building the design versus a build it and see mentality *Electrical Overstress (EOS)* Steven H. Voldman,2013-08-27 Electrical Overstress EOS continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures The text provides a clear picture of EOS phenomena EOS origins EOS sources EOS physics EOS failure mechanisms and EOS on chip and system design It provides an illuminating insight into the sources of EOS in manufacturing integration of on chip and system level EOS protection networks followed by examples in specific technologies circuits and chips The book is unique in covering the EOS manufacturing issues from on chip design and electronic design automation to factory level EOS program management in today s modern world Look inside for extensive

coverage on Fundamentals of electrical overstress from EOS physics EOS time scales safe operating area SOA to physical models for EOS phenomena EOS sources in today s semiconductor manufacturing environment and EOS program management handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices circuits and system Discussion of how to distinguish between EOS events and electrostatic discharge ESD events e g such as human body model HBM charged device model CDM cable discharge events CDM charged board events CBE to system level IEC 61000 4 2 test events EOS protection on chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards PCB and manufacturing equipment Examples of EOS issues in state of the art digital analog and power technologies including CMOS LDMOS and BCD EOS design rule checking DRC LVS and ERC electronic design automation EDA and how it is distinct from ESD EDA systems EOS testing and qualification techniques and Practical off chip ESD protection and system level solutions to provide more robust systems Electrical Overstress EOS Devices Circuits and Systems is a continuation of the author s series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano electronic era **Low-power HF Microelectronics** Gerson A. S. Machado,1996 This book brings together innovative modelling simulation and design techniques in CMOS SOI GaAs and BJT to achieve successful high yield manufacture for low power high speed and reliable by design analogue and mixed mode integrated systems ESD Design and Analysis Handbook James E. Vinson,Joseph C. Bernier,Gregg D. Croft,Juin Jei Liou,2012-12-06 ESD Design and Analysis Handbook presents an overview of ESD as it effects electronic circuits and provides a concise introduction for students engineers circuit designers and failure analysts This handbook is written in simple terms and is filled with practical advice and examples to illustrate the concepts presented While this treatment is not exhaustive it presents many of the most important areas of the ESD problem and suggests methods for improving them The key topics covered include the physics of the event failure analysis protection characterization and simulation techniques The book is intended as both an introductory text on ESD and a useful reference tool to draw on as the reader gains experience The authors have tried to balance the level of detail in the ESD Design and Analysis Handbook against the wealth of literature published on ESD every year To that end each chapter has a topical list of references to facilitate further in depth study **Introduction to VLSI Systems** Ming-Bo Lin,2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder problems requires fundamental understanding

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