

SEQUENTIAL OPTIMIZATION
OF ASYNCHRONOUS
AND SYNCHRONOUS
FINITE-STATE MACHINES
Algorithms and Tools

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K l u w e r A c a d e m i c P u b l i s h e r s

Sequential Optimization Of Asynchronous And Synchronous Finite State Machines Algorithms And Tools

Robert Fuhrer



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Sequential Optimization of Asynchronous and Synchronous Finite-State Machines Robert M. Fuhrer, Steven M. Nowick, 2012-12-06 Asynchronous or unclocked digital systems have several potential advantages over their synchronous counterparts In particular they address a number of challenging problems faced by the designers of large scale synchronous digital systems power consumption worst case timing constraints and engineering and design reuse issues associated with the use of a fixed rate global clock Moreover while for synchronous systems these problems are exacerbated by increasing system size asynchronous systems promise to scale more gracefully Sequential Optimization of Asynchronous and Synchronous Finite State Machines Algorithms and Tools makes three contributions to the field of sequential optimization for finite state machines 1 it introduces several new provably optimal algorithms for the synthesis and optimization of asynchronous finite state machines FSMs 2 it presents practical software implementations of each of these algorithms and 3 it introduces a complete new CAD package called MINIMALIST binding these tools into a state of the art technology independent synthesis path for burst mode asynchronous circuits Throughout this book real world industrial designs are used as benchmark circuits to validate the usefulness of the tools As an additional benefit some of the theory and tools also provide new methods for the optimization of synchronous FSMs

Sequential Optimization of Asynchronous and Synchronous Finite-state Machines Robert Fuhrer, 1999 Logic Synthesis and Verification Soha Hassoun, Tsutomu Sasao, 2012-12-06 Research and development of logic synthesis and verification have matured considerably over the past two decades Many commercial products are available and they have been critical in harnessing advances in fabrication technology to produce today s plethora of electronic components While this maturity is assuring the advances in fabrication continue to seemingly present unwieldy challenges Logic Synthesis and Verification provides a state of the art view of logic synthesis and verification It consists of fifteen chapters each focusing on a distinct aspect Each chapter presents key developments outlines future challenges and lists essential references Two unique features of this book are technical strength and comprehensiveness The book chapters are written by twenty eight recognized leaders in the field and reviewed by equally qualified experts The topics collectively span the field Logic Synthesis and Verification fills a current gap in the existing CAD literature Each chapter contains essential information to study a topic at a great depth and to understand further developments in the field The book is intended for seniors graduate students researchers and developers of related Computer Aided Design CAD tools From the foreword The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book Their innovative work contributed to design automation tools that permanently changed the course of electronic design by Aart J de Geus Chairman and CEO Synopsys Inc

Design Automation of Real-Life Asynchronous Devices and Systems Alexander Taubin, Jordi Cortadella, Luciano Lavagno, 2007 The number of gates on a chip is quickly growing toward and beyond the one billion mark Keeping all the gates running at

the beat of a single or a few rationally related clocks is becoming impossible In static timing analysis process variations and signal integrity issues stretch the timing margins to the point where they become too conservative and result in significant overdesign Importance and difficulty of such problems push some developers to once again turn to asynchronous alternatives However the electronics industry for the most part is still reluctant to adopt asynchronous design with a few notable exceptions due to a common belief that we still lack a commercial quality Electronic Design Automation tools similar to the synchronous RTL to GDSII flow for asynchronous circuits The purpose of this paper is to counteract this view by presenting design flows that can tackle large designs without significant changes with respect to synchronous design flow We are limiting ourselves to four design flows that we believe to be closest to this goal We start from the Tangram flow because it is the most commercially proven and it is one of the oldest from a methodological point of view The other three flows Null Convention Logic de synchronization and gate level pipelining could be considered together as asynchronous re implementations of synchronous RTL or gate level specifications The main common idea is substituting the global clocks by local synchronizations Their most important aspect is to open the possibility to implement large legacy synchronous designs in an almost push button manner where all asynchronous machinery is hidden so that synchronous RTL designers do not need to be re educated These three flows offer a trade off from very low overhead almost synchronous implementations to very high performance extremely robust dual rail pipelines

Dissertation Abstracts International ,2000 **Digest of Technical Papers** ,1999 Photonics Applications in Industry and Research IV ,2005 American Doctoral Dissertations ,2000 *Scientific and Technical Aerospace Reports* ,1995 **Logic Synthesis for FPGA-Based Mealy Finite State Machines** Alexander Barkalov,Larysa Titarenko,Kazimierz Krzywicki,2024-12-04 This book is devoted to the logic synthesis of field programmable gate array FPGA based circuits of Mealy finite state machines FSM Three new methods of state assignment are proposed which allows obtaining FSM circuits required minimum amount of internal chip resources Logic Synthesis for FPGA Based Mealy Finite State Machines Structural Decomposition in Logic Design contains several original synthesis and optimization methods based on the structural decomposition of FPGA based FSM circuits developed by the authors To optimize FSM circuits the authors introduce the use of three methods of state assignment twofold extended and composite These methods allow for the creation of two or three level architectures of FSM circuits The authors also demonstrate how the proposed methods FSM architectures and synthesis methods can replace known solutions based on either functional decomposition or classical methods of structural decomposition The authors also show how these architectures have regular systems of interconnections and demonstrate positive features compared to methods based on functional decomposition including producing circuits with fewer elements that are faster and consume less power than their counterparts The book includes experimental results proving the efficiency of the proposed solutions and compares the numbers in Look up Tables LUTs showing the performance maximum operating frequency and power consumption for

various methods of state assignment The audience for this book is students researchers and engineers specializing in computer science engineering electronics and telecommunications It will be especially useful for engineers working within the scope of algorithms hardware based software accelerators and control units and systems based on the use of FPGAs

Embedded Systems Handbook Richard Zurawski, 2018-09-03 Considered a standard industry resource the Embedded Systems Handbook provided researchers and technicians with the authoritative information needed to launch a wealth of diverse applications including those in automotive electronics industrial automated systems and building automation and control Now a new resource is required to report on current developments and provide a technical reference for those looking to move the field forward yet again Divided into two volumes to accommodate this growth the Embedded Systems Handbook Second Edition presents a comprehensive view on this area of computer engineering with a currently appropriate emphasis on developments in networking and applications Those experts directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews that explore cutting edge developments and deployments and identify potential trends This first self contained volume of the handbook Embedded Systems Design and Verification is divided into three sections It begins with a brief introduction to embedded systems design and verification It then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Those interested in taking their work with embedded systems to the network level should complete their study with the second volume Network Embedded Systems

Synthesis of Finite State Machines Tiziano Villa, Timothy Kam, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli, 2012-12-06

Synthesis of Finite State Machines Logic Optimization is the second in a set of two monographs devoted to the synthesis of Finite State Machines FSMs The first volume Synthesis of Finite State Machines Functional Optimization addresses functional optimization whereas this one addresses logic optimization The result of functional optimization is a symbolic description of an FSM which represents a sequential function chosen from a collection of permissible candidates Logic optimization is the body of techniques for converting a symbolic description of an FSM into a hardware implementation The mapping of a given symbolic representation into a two valued logic implementation is called state encoding or state assignment and it impacts heavily area speed testability and power consumption of the realized circuit The first part of the book introduces the relevant background presents results previously scattered in the literature on the computational complexity of encoding problems and surveys in depth old and new approaches to encoding in logic synthesis The second part of the book presents two main results about symbolic minimization a new procedure to find minimal two level symbolic covers under face dominance and disjunctive constraints and a unified frame to check encodability of encoding constraints and find codes of minimum length that satisfy them The third part of the book introduces

generalized prime implicants GPIs which are the counterpart in symbolic minimization of two level logic to prime implicants in two valued two level minimization GPIs enable the design of an exact procedure for two level symbolic minimization based on a covering step which is complicated by the need to guarantee encodability of the final cover A new efficient algorithm to verify encodability of a selected cover is presented If a cover is not encodable it is shown how to augment it minimally until an encodable superset of GPIs is determined To handle encodability the authors have extended the frame to satisfy encoding constraints presented in the second part The covering problems generated in the minimization of GPIs tend to be very large Recently large covering problems have been attacked successfully by representing the covering table with binary decision diagrams BDD In the fourth part of the book the authors introduce such techniques and extend them to the case of the implicit minimization of GPIs where the encodability and augmentation steps are also performed implicitly Synthesis of Finite State Machines Logic Optimization will be of interest to researchers and professional engineers who work in the area of computer aided design of integrated circuits

Computer Information Systems and Industrial Management Khalid Saeed, Jiří Dvorský, 2020-05-22 This book constitutes the proceedings of the 19th International Conference on Computer Information Systems and Industrial Management Applications CISIM 2020 held in Białystok Poland in October 2020 Due to the COVID 19 pandemic the conference has been postponed to October 2020 The 40 full papers presented together with 5 abstracts of keynotes were carefully reviewed and selected from 62 submissions The main topics covered by the chapters in this book are biometrics security systems multimedia classification and clustering industrial management Besides these the reader will find interesting papers on computer information systems as applied to wireless networks computer graphics and intelligent systems The papers are organized in the following topical sections biometrics and pattern recognition applications computer information systems and security industrial management and other applications machine learning and high performance computing modelling and optimization

Seventh International Symposium on Asynchronous Circuits and Systems : ASYNC 2001, 2001 **7th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC 2001)**, 2001 Comprises 20 papers selected for presentation at the Async 2001 conference in March 2001 as well as three invited presentations from industry researchers Papers were divided into seven sessions systems arithmetic experiments synthesis and verification handshaking communication architecture and performance analysis and optimization The invited talks are titled Asynchronous Design and the Pursuit of Low Power Where Are the Async Millionaires and Testing Asynchronous Circuits Help Is on the Way Indexed by author but not by subject c Book News Inc

Logic Synthesis for FPGA-Based Control Units Alexander Barkalov, Larysa Titarenko, Kamil Mielcarek, Sławomir Chmielewski, 2020-01-08 This book focuses on control units which are a vital part of modern digital systems and responsible for the efficiency of controlled systems The model of a finite state machine FSM is often used to represent the behavior of a control unit As a rule control units have irregular structures that make it impossible to design their logic circuits using the standard library cells Design

methods depend strongly on such factors as the FSM used specific features of the logic elements implemented in the FSM logic circuit and the characteristics of the control algorithm to be interpreted This book discusses Moore and Mealy FSMs implemented with FPGA chips including look up table elements LUT and embedded memory blocks EMB It is crucial to minimize the number of LUTs and EMBs in an FSM logic circuit as well as to make the interconnections between the logic elements more regular and various methods of structural decompositions can be used to solve this problem These methods are reduced to the presentation of an FSM circuit as a composition of different logic blocks the majority of which implement systems of intermediate logic functions different and much simpler than input memory functions and FSM output functions The structural decomposition results in multilevel FSM circuits having fewer logic elements than equivalent single level circuits The book describes well known methods of structural decomposition and proposes new ones examining their impact on the final amount of hardware in an FSM circuit It is of interest to students and postgraduates in the area of Computer Science as well as experts involved in designing digital systems with complex control units The proposed models and design methods open new possibilities for creating logic circuits of control units with an optimal amount of hardware and regular interconnections

Optimization of Automated Software Testing Using Meta-Heuristic Techniques Manju Khari, Deepti Bala Mishra, Biswaranjan Acharya, Ruben Gonzalez Crespo, 2022-09-26 This book provides awareness of different evolutionary methods used for automatic generation and optimization of test data in the field of software testing While the book highlights on the foundations of software testing techniques it also focuses on contemporary topics for research and development This book covers the automated process of testing in different levels like unit level integration level performance level evaluation of testing strategies testing in security level optimizing test cases using various algorithms and controlling and monitoring the testing process etc This book aids young researchers in the field of optimization of automated software testing provides academics with knowledge on the emerging field of AI in software development and supports universities research centers and industries in new projects using AI in software testing Supports the advancement in the artificial intelligence used in software development Advances knowledge on artificial intelligence based metaheuristic approach in software testing Encourages innovation in traditional software testing field using recent artificial intelligence

IEEE, ACM International Conference on Computer Aided Design International Conference on Computer Aided Design. Institute of Electrical and Electronics Engineers, 2000, San José, Calif., 2000

Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for

manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals
American Book Publishing Record ,2001

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Introduction

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