Modeling, Design, and Verification for the Analog Front-End of a MEMS-Based Parallel Scanning-Probe Storage Device

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Abstract-We present an integrated analog front-end (AFE) for the read-channel of a parallel scanning-probe storage device. The read/write element is based on an array of microfabricated silicon cantilevers equipped with heating elements to form nanometer-sized indentations in a polymer surface using integral atomic-force microscope (AFM) tips. An accurate cantilever model based on the combination of a thermal/electrical lumped-element model and a behavioral model of the electrostatic/mechanical part are introduced. The behavioral model of the electrostatic/mechanical part is automatically generated from a full finite-element model (FEM). The model is completely implemented in Verilog-A. and was used to co-develop the integrated analog front-end circuitry together with the read/write cantilever. The cantilever model and the analog front-end were simulated together and the results were experimentally verified. The approach chosen is well suited for system-level simulation and verification/extraction in a design environment based on standard EDA tools.

Index Terms—Analog integrated circuits, integrated circuit modeling, MEMS interface circuits, model-order reduction, multidomain modeling, nanotechnology, sensor interface circuits.

I. INTRODUCTION

ULTRAHIGH storage densities of 1 Tb/in² or higher can be achieved by using local-probe techniques to write, read back, and erase data in very thin polymer films. The thermomechanical scanning-probe-based data-storage concept, internally dubbed "millipede" [1], [2], combines ultrahigh density, small form factor, and high data rates. High data rates are achieved by parallel operation of large 2-D arrays with thousands of micro/ nanomechanical cantilevers/tips that can be batch-fabricated by silicon surface-micromachining techniques. Fig. 1 illustrates the "millipede" concept.

The high precision required to navigate the storage medium over the probe tips is achieved by MEMS-based 2/g actuators that position the large arrays of probe tips for parallel write/read/

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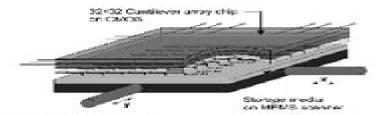


Fig. 1. The "millipede" concept.

erase operations. Thermomechanical writing is achieved by applying a local force through the cantilever/tip to the polymer layer and simultaneously softening the polymer layer by local heating. To read the written information, the same cantilever is used to scan the surface. The change in the thermal flow between a second heating element and the medium surface leads to a change in the electrical resistance of the heating element (see Fig. 2) [3].

The parallel operation of hundreds of cantilevers makes the CMOS integration of the analog front-end (AFE) imperative. To this end, a 3-D assembling technology has been developed to transfer the cantilevers onto the CMOS read-out circuitry [4]. The small relative resistance change $(\Delta R/R < 10^{-6})$ for a typical indentation) renders the design of the AFE's read-channel a challenging task. This paper describes the design of the critical input stage of the read-channel based on co-simulation of the AFE circuitry and a multi-domain cantilever model. The resulting read-channel is the centerpiece of a 32-channel AFE chip [5]. Section II of the paper focuses on the model of the cantilever and Section III presents its experimental verification. Section IV gives the details on the model-based design and optimization of the critical first stage in the read-channel. Experimental results obtained with the complete 32-channel chip that was wirebonded to a cantilever array are also shown. Section V summarizes the paper.

II. VERILOG-A CANTLEVER MODEL

The AFE for the thermomechanical storage device is in essence a transducer interface circuit. As described above, information is stored in the mechanical topography of a thin polymer film. The micromechanical cantilever acts as a transducer to convert topographical variations into electrical energy during the read process, and vice versa during the write process.

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nite the state space traversal will eventually terminate with a de nite verdict on the property that is being validated Equally helpful is the fact that in case the property is invidated the model checker will return a counterexample a feature that greatly facilitates fault identification On the downside the time it takes to obtain a verdict may be very long if the state space is large and the type of properties that can be validated is restricted to a logic of rather limited expressiveness Checking Software Dragan Bosnacki, Stefan Leue, 2003-08-01 The SPIN workshop series brings together researchers and practitioners int ested in explicit state model checking technology as it is applied to the veri tion of software systems Since 1995 when the SPIN workshop series was instigated SPIN workshops have been held on an annual basis at Montr eal 1995 New Brunswick 1996 Enschede 1997 Paris 1998 Trento 1999 Toulouse 1999 Stanford 2000 and Toronto 2001 Whilethe rstSPINworkshopwasastand aloneevent later workshopshavebeenorganizedasmoreorlesscloselya liatedeventswithlarger conferences in particular with CAV 1996 TACAS 1997 FORTE PSTV 1998 FLOC 1999 World Congress on Formal Methods 1999 FMOODS 2000 and ICSE 2001 This year SPIN 2002 was held as a satellite event of ETAPS 2002 the European Joint Conferences on Theory and Practice of Software The co location of SPIN workshops with conferences has proven to be very successful and has helped to disseminate SPIN model checking technology to wider audiences Since 1999 the proceedings of the SPIN workshops have appeared in Springer Verlag's Lecture Notes in Computer Science series The history of successful SPIN workshops is evidence for the maturing of model checking technology not only in the hardware domain but increasingly also in the software area While in earlier years algorithms and tool development 1 around the SPIN model checker were the focus of this workshop series the scopehasrecentlywidenedtoincludemoregeneral approaches to software model checking Current research in this area concentrates not so much on completely verifying system models butratheronanalyzingsourcecodeinordertodiscover software faults Web-Age Information Management Bin Cui, Nan Zhang, Jianliang Xu, Xiang Lian, Dexi Liu, 2016-05-31 This two volume set LNCS 9658 and 9659 constitutes the thoroughly refereed proceedings of the 17th International Conference on Web Age Information Management WAIM 2016 held in Nanchang China in June 2016 The 80 full research papers presented together with 8 demonstrations were carefully reviewed and selected from 266 submissions. The focus of the conference is on following topics data mining spatial and temporal databases recommender systems graph data management information retrieval privacy and trust query processing and optimization social media big data analytics and distributed and cloud computing **System Analysis and Modeling:** Models and Reusability Daniel Amyot, Pau Fonseca i Casas, Gunter Mussbacher, 2014-09-24 This book constitutes the refereed papers of the proceedings of the 8th International Conference on System Analysis and Modeling SAM 2014 held in Valencia Spain in September 2014 The 18 full papers and the 3 short papers presented together with 2 keynotes were carefully reviewed and selected from 71 submissions. The contributions are organized in topical sections named reuse availability safety and optimization sequences and interactions testing metrics constraints and repositories and SDL and V V

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Table of Contents Modeling And Verification Of Parallel Procebes

- 1. Understanding the eBook Modeling And Verification Of Parallel Procebes
 - The Rise of Digital Reading Modeling And Verification Of Parallel Procebes
 - Advantages of eBooks Over Traditional Books
- 2. Identifying Modeling And Verification Of Parallel Procebes
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
- 3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Modeling And Verification Of Parallel Procebes
 - User-Friendly Interface
- 4. Exploring eBook Recommendations from Modeling And Verification Of Parallel Procebes
 - Personalized Recommendations
 - Modeling And Verification Of Parallel Procebes User Reviews and Ratings
 - Modeling And Verification Of Parallel Procebes and Bestseller Lists

- 5. Accessing Modeling And Verification Of Parallel Procebes Free and Paid eBooks
 - Modeling And Verification Of Parallel Procebes Public Domain eBooks
 - Modeling And Verification Of Parallel Procebes eBook Subscription Services
 - Modeling And Verification Of Parallel Procebes Budget-Friendly Options
- 6. Navigating Modeling And Verification Of Parallel Procebes eBook Formats
 - ∘ ePub, PDF, MOBI, and More
 - Modeling And Verification Of Parallel Procebes Compatibility with Devices
 - Modeling And Verification Of Parallel Procebes Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Modeling And Verification Of Parallel Procebes
 - Highlighting and Note-Taking Modeling And Verification Of Parallel Procebes
 - Interactive Elements Modeling And Verification Of Parallel Procebes
- 8. Staying Engaged with Modeling And Verification Of Parallel Procebes
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Modeling And Verification Of Parallel Procebes
- 9. Balancing eBooks and Physical Books Modeling And Verification Of Parallel Procebes
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Modeling And Verification Of Parallel Procebes
- 10. Overcoming Reading Challenges
 - o Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Modeling And Verification Of Parallel Procebes
 - Setting Reading Goals Modeling And Verification Of Parallel Procebes
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Modeling And Verification Of Parallel Procebes
 - Fact-Checking eBook Content of Modeling And Verification Of Parallel Procebes
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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