Reuse Techniques for VLSI Design

Edited by Ralf Seepold and Arno Kunzmann

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Reuse Techniques For Vlsi Design

Workshop Reuse Techniques for VLSI Design. 2, 1998, Karlsruhe

Reuse Techniques For Vlsi Design:

Reuse Techniques for VLSI Design Ralf Seepold, Arno Kunzmann, 1999-03-31 Reuse Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since design reuse must not be restricted to digital components mixed signal and analog reuse approaches are also presented In parallel to the digital domain this area covers research in reuse database design Design verification and legal aspects are two important topics that are closely related to the realization of design reuse These hot topics are covered by presentations that finalize the survey of outstanding research development and application of design reuse for SoC design Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI ASIC design

Reuse Techniques for VLSI Design Ralf Seepold,Arno Kunzmann,2012-12-06 Reuse Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since design reuse must not be restricted to digital components mixed signal and analog reuse approaches are also presented In parallel to the digital domain this area covers research in reuse database design Design verification and legal aspects are two important topics that are closely related to the realization of design reuse These hot topics are covered by presentations that finalize the survey of outstanding research development and application of design reuse for SoC design Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI ASIC design

topic of research but a real industrial necessity in the microelectronic domain and thus driving the competitiveness of relevant areas like for example telecommunication or automotive Most companies have already dedicated a department or a central unit that transfer design reuse into reality All main EDA conferences include a track to the topic and even specific conferences have been established in this area both in the USA and in Europe Virtual Components Design and Reuse presents a selection of articles giving a mature and consolidated perspective to design reuse from different points of view The authors stem from all relevant areas research and academia IP providers EDA vendors and industry Some classical topics in design reuse like specification and generation of components IP retrieval and cataloguing or interface customisation are revisited and discussed in depth Moreover new hot topics are presented among them IP quality platform based reuse software IP IP security business models for design reuse and major initiatives like the MEDEA EDA Roadmap Level Design Model with Reuse of System IP Patrizia Cavalloro, Christophe Gendarme, Klaus Kronlöf, Jean Mermet, J. van Sas, Kari Tiensyrjä, Nikolaos Voros, 2007-05-08 This book addresses system design providing a framework for assessing and developing system design practices that observe and utilise reuse of system design know how The know how accumulated in the companies represents an intellectual asset or property IP System-on-Chip Methodologies & Design Languages Peter J. Ashenden, Jean Mermet, Ralf Seepold, 2013-03-14 System on Chip Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly Advances in Case-Based Reasoning Susan Craw, Alun Preece, 2003-08-02 The papers collected in this evolving field volume were presented at the 6th European C ference on Case Based Reasoning ECCBR 2002 held at The Robert Gordon University in Aberdeen UK This conference followed a series of very succe ful well established biennial European workshops held in Trento Italy 2000 Dublin Ireland 1998 Lausanne Switzerland 1996 and Paris France 1994 after the initial workshop in Kaiserslautern Germany 1993 These meetings have a history of attracting rst class European and international researchers and practitioners in the years interleaving with the biennial international co terpart ICCBR the 4th ICCBR Conference was held in Vancouver Canada in 2001 Proceedings of ECCBR and ICCBR conferences are traditionally published by Springer Verlag in their LNAI series Case Based Reasoning CBR is an AI problem solving approach where pr lems are solved by retrieving and reusing solutions from similar previously solved problems and possibly revising the retrieved solution to re ect di erences tween the new and retrieved problems Case knowledge stores the previously solved problems and is the main knowledge source of a CBR system A main focus of CBR research is the representation acquisition and maintenance of case knowledge Recently other knowledge sources have been recognized as important indexing similarity and adaptation knowledge Signi cant knowledge engine ing e ort may be needed for these and so the representation acquisition and

maintenance of CBR knowledge more generally have become important Intellectual Property Protection in VLSI

Designs Gang Qu, Miodrag Potkonjak, 2007-05-08 Intellectual Property Protection in VLSI Designs Theory and Practice provides an overview of the security problems in modern VLSI design with a detailed treatment of our newly developed constraint based protection paradigm for the protection of VLSI design IPs from FPGA design to standard cell placement from high level synthesis solutions to gate level netlist place and rout and from advanced CAD tools to physical design algorithms The problem of VLSI design IP protection is much more challenging than the protection of multimedia contents or software and our protection paradigm is also conceptually different from the state of the art approaches in those domains Intellectual Property Protection in VLSI Designs Theory and Practice contains the mathematical foundations for the developed IP protection paradigm detailed pseudo code and descriptions of its many techniques numerous examples and experimental validation on well known benchmarks and clear explanations and comparisons of the many protection methods

Formal Methods in Circuit Design Victoria Stavridou,1993-07-22 Graduate level account of hardware verification and algebraic specification

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