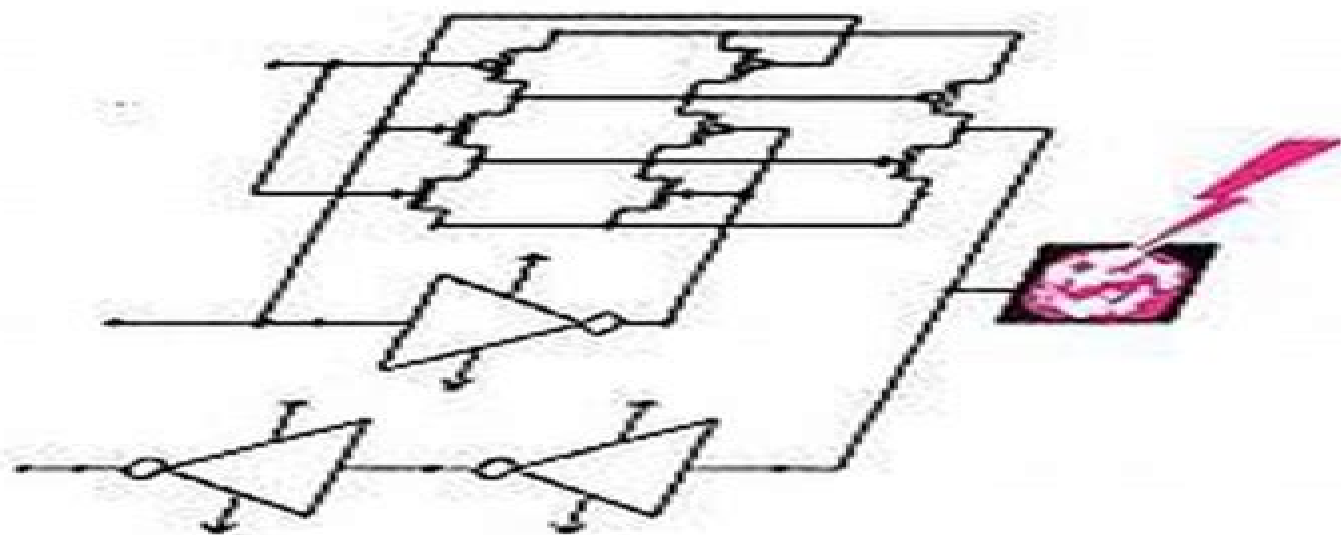
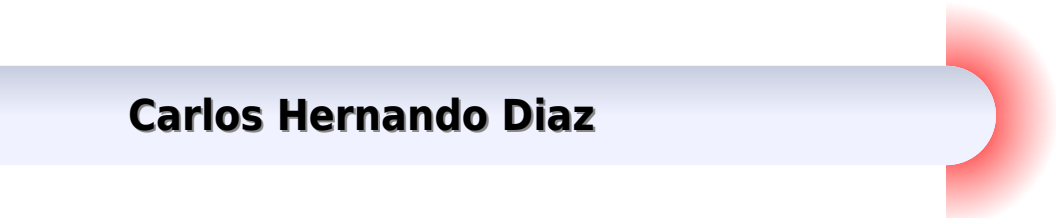

MODELING OF ELECTRICAL OVERSTRESS IN INTEGRATED CIRCUITS



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Modeling Of Electrical Overstress In Integrated Circuits

Carlos Hernando Diaz



Modeling Of Electrical Overstress In Integrated Circuits:

Modeling of Electrical Overstress in Integrated Circuits Carlos H. Diaz, Sung-Mo (Steve) Kang, Charvaka Duvvury, 2012-12-06 Electrical overstress EOS and Electrostatic discharge ESD pose one of the most dominant threats to integrated circuits ICs These reliability concerns are becoming more serious with the downward scaling of device feature sizes Modeling of Electrical Overstress in Integrated Circuits presents a comprehensive analysis of EOS ESD related failures in I O protection devices in integrated circuits The design of I O protection circuits has been done in a hit or miss way due to the lack of systematic analysis tools and concrete design guidelines In general the development of on chip protection structures is a lengthy expensive iterative process that involves tester design fabrication testing and redesign When the technology is changed the same process has to be repeated almost entirely This can be attributed to the lack of efficient CAD tools capable of simulating the device behavior up to the onset of failure which is a 3 D electrothermal problem For these reasons it is important to develop and use an adequate measure of the EOS robustness of integrated circuits in order to address the on chip EOS protection issue Fundamental understanding of the physical phenomena leading to device failures under ESD EOS events is needed for the development of device models and CAD tools that can efficiently describe the device behavior up to the onset of thermal failure Modeling of Electrical Overstress in Integrated Circuits is for VLSI designers and reliability engineers particularly those who are working on the development of EOS ESD analysis tools CAD engineers working on development of circuit level and device level electrothermal simulators will also benefit from the material covered This book will also be of interest to researchers and first and second year graduate students working in semiconductor devices and IC reliability fields

Modeling and Simulation of Electrical Overstress Failures in Input/output Protection Devices of Integrated Circuits Carlos Hernando Diaz, 1993 It is proposed in this thesis that a measure to determine the electrical overstress EOS hardness of integrated circuits with respect to EOS electrostatic discharge ESD can be measured in terms of the power vs time to failure relationship power profile and the current vs time to failure relationship current profile A new nonlinear mixed 2D 1D thermal simulator iTSIM was developed in order to understand and quantify the sensitivity of the power profiles with respect to major thermal parameters of the integrated circuit IC Protection devices with different layout parameters were fabricated and experimentally characterized for EOS Experimental data indicate that these devices fail with a poly gate filament in the drain edge when subjected to ESD or short duration EOS events while extensive device damage is observed for long duration EOS events revealing onset of thermal runaway Two dimensional 2D device level electrothermal simulations are used to develop qualitative analysis of both the physical mechanisms leading to device failure and the dependencies of the failure thresholds power and current profiles on the layout parameters Results from this study coupled with heat removal considerations led to a design guideline for source contact placement that is expected to improve the failure thresholds for I O protection devices of CMOS ICs with grounded substrate Thermal instability of an electrically

stressed circuit or device is shown to be the result of either thermally induced negative differential resistance NDR in resistive regions or junction second breakdown Under typical ESD EOS stress events transient in nature the temperature at which thermal instability takes place depends on the level of the stress current In semiconductor junctions reverse biased by an EOS event second breakdown is shown to happen at the time when thermal carrier generation becomes high enough to offset the effects of the mobility degradation and the reduction of the impact ionization rates Under these circumstances the time for the onset of second breakdown is shown to depend on the device's geometry and the level of power dissipation Circuit level electrothermal models are introduced for resistors diodes and bipolar and MOS transistors they are capable of describing device behaviour up into thermal runaway or second breakdown

Abstract shortened by UMI *On-Chip ESD Protection for Integrated Circuits* Albert Z.H. Wang, 2006-01-03 This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer's perspective On Chip ESD Protection for Integrated Circuits An IC Design Perspective provides both fundamental and advanced materials needed by a circuit designer for designing ESD protection circuits including Testing models and standards adopted by U S Department of Defense EIA JEDEC ESD Association Automotive Electronics Council International Electrotechnical Commission etc ESD failure analysis protection devices and protection of sub circuits Whole chip ESD protection and ESD to circuit interactions Advanced low parasitic compact ESD protection structures for RF and mixed signal IC's Mixed mode ESD simulation design methodologies for design prediction ESD to circuit interactions and more Many real world ESD protection circuit design examples are provided The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field

Electrical Overstress (EOS) Steven H. Voldman, 2013-08-27 Electrical Overstress EOS continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This book teaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures The text provides a clear picture of EOS phenomena EOS origins EOS sources EOS physics EOS failure mechanisms and EOS on chip and system design It provides an illuminating insight into the sources of EOS in manufacturing integration of on chip and system level EOS protection networks followed by examples in specific technologies circuits and chips The book is unique in covering the EOS manufacturing issues from on chip design and electronic design automation to factory level EOS program management in today's modern world Look inside for extensive coverage on Fundamentals of electrical overstress from EOS physics EOS time scales safe operating area SOA to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment and EOS program management handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices circuits and system Discussion of how to distinguish between EOS events and electrostatic discharge ESD events e.g. such as human body model HBM charged device model CDM cable discharge events CDM charged board events CBE to system level IEC 61000 4 2 test events EOS protection on chip design practices and how

they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards PCB and manufacturing equipment Examples of EOS issues in state of the art digital analog and power technologies including CMOS LDMOS and BCD EOS design rule checking DRC LVS and ERC electronic design automation EDA and how it is distinct from ESD EDA systems EOS testing and qualification techniques and Practical off chip ESD protection and system level solutions to provide more robust systems Electrical Overstress EOS Devices Circuits and Systems is a continuation of the author s series of books on ESD protection It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano electronic era

Simulation Methods for ESD Protection Development

Harald Gossner,Kai Esmark,Wolfgang Stadler,2003-10-16 Simulation Methods for ESD Protection Development looks at the integration of new techniques into a comprehensive development flow which is now available due advances made in the field during the recent years These findings allow for an early stable ESD concept at a very early stage of the technology development which is essential now development cycles have been reduced The book also offers ways of increasing the optimization and control of the technology concerning performance thus making the process more cost effective and increasingly efficient This title provides a guide through the latest research and technology presenting the ESD protection development methodology This is based on a combination of process device and circuit stimulation and addresses the optimization of the industry critical issue reduced development cycles Written to address the needs of the ESD engineer this text is required reading by all industry practitioners and researchers and students within this field The FIRST Extensive overview on the subject of ESD simulation Addresses the industry critical issue of reduced development cycles and provides solutions Presents the latest research in the field with high practical relevance and its results

Integrated Circuit Test Engineering Ian A. Grout,2005-12-08 Taking a three pronged approach test engineering from traditional test design and manufacturing view points Integrated Circuit Test Engineering encapsulates the subject as it stands today After introductory background from basic testing rules to trends in technology the reader learns about fabrication processes a complete range of detailed tests and procedures how to design for testability fault simulation automatic test equipment and the economics of testing The text includes Worked examples and exercises well organized references and bibliography An introduction to the use of various software and languages such as MATLAB Spice Verilog HDL and VHDL A series of experiments based on material downloaded from springeronline com showing how to construct a hardware test arrangement for MS Windows PCs This book is a practical tool for advanced undergraduate and graduate electronic engineering students a resource for their tutors and a guide for the practising electronic engineer

On-Chip Electro-Static Discharge (ESD) Protection for

Radio-Frequency Integrated Circuits Qiang Cui,Juin J. Liou,Jean-Jacques Hajjar,Javier Salcedo,Yuanzhong

Zhou,Parthasarathy Srivatsan,2015-03-10 This book enables readers to design effective ESD protection solutions for all mainstream RF fabrication processes GaAs pHEMT SiGe HBT CMOS The new techniques introduced by the authors have

much higher protection levels and much lower parasitic effects than those of existing ESD protection devices The authors describe in detail the ESD phenomenon as well as ESD protection fundamentals standards test equipment and basic design strategies Readers will benefit from realistic case studies of ESD protection for RFICs and will learn to increase significantly modern RFICs ESD safety level while maximizing RF performance

Electrothermal Analysis of VLSI Systems Yi-Kan Cheng, Ching-Han Tsai, Chin-Chi Teng, Sung-Mo (Steve) Kang, 2005-12-01 This useful book addresses electrothermal problems in modern VLSI systems It discusses electrothermal phenomena and the fundamental building blocks that electrothermal simulation requires The authors present three important applications of VLSI electrothermal analysis temperature dependent electromigration diagnosis cell level thermal placement and temperature driven power and timing analysis

Field-Programmable Analog Arrays Edmund Pierzchala, Glenn Gulak, Leon Chua, Angel Rodríguez-Vázquez, 2013-06-29 Field Programmable Analog Arrays brings together in one place important contributions and up to date research results in this fast moving area Field Programmable Analog Arrays serves as an excellent reference providing insight into some of the most challenging research issues in the field

Transient-Induced Latchup in CMOS Integrated Circuits Ming-Dou Ker, Sheng-Fu Hsu, 2009-07-23 The book all semiconductor device engineers must read to gain a practical feel for latchup induced failure to produce lower cost and higher density chips Transient Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup explaining the critical issues that have resurfaced for CMOS technologies Once readers can gain an understanding of the standard practices for TLU Ker and Hsu discuss the physical mechanism of TLU under a system level ESD test while introducing an efficient component level TLU measurement setup The authors then present experimental methodologies to extract safe and area efficient compact layout rules for latchup prevention including layout rules for I O cells internal circuits and between I O and internal circuits The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18 micrometer 1.8V/3.3V silicided CMOS process Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time to market Written by experts with real world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system level ESD and EFT tests This book is essential for practicing engineers involved in IC design IC design management system and application design reliability and failure analysis Undergraduate and postgraduate students specializing in CMOS circuit design and layout will find this book to be a valuable introduction to real world industry problems and a key reference during the course of their careers

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Table of Contents Modeling Of Electrical Overstress In Integrated Circuits

1. Understanding the eBook Modeling Of Electrical Overstress In Integrated Circuits
 - The Rise of Digital Reading Modeling Of Electrical Overstress In Integrated Circuits
 - Advantages of eBooks Over Traditional Books
2. Identifying Modeling Of Electrical Overstress In Integrated Circuits
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Modeling Of Electrical Overstress In Integrated Circuits
 - User-Friendly Interface
4. Exploring eBook Recommendations from Modeling Of Electrical Overstress In Integrated Circuits
 - Personalized Recommendations
 - Modeling Of Electrical Overstress In Integrated Circuits User Reviews and Ratings
 - Modeling Of Electrical Overstress In Integrated Circuits and Bestseller Lists

5. Accessing Modeling Of Electrical Overstress In Integrated Circuits Free and Paid eBooks
 - Modeling Of Electrical Overstress In Integrated Circuits Public Domain eBooks
 - Modeling Of Electrical Overstress In Integrated Circuits eBook Subscription Services
 - Modeling Of Electrical Overstress In Integrated Circuits Budget-Friendly Options
6. Navigating Modeling Of Electrical Overstress In Integrated Circuits eBook Formats
 - ePub, PDF, MOBI, and More
 - Modeling Of Electrical Overstress In Integrated Circuits Compatibility with Devices
 - Modeling Of Electrical Overstress In Integrated Circuits Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Modeling Of Electrical Overstress In Integrated Circuits
 - Highlighting and Note-Taking Modeling Of Electrical Overstress In Integrated Circuits
 - Interactive Elements Modeling Of Electrical Overstress In Integrated Circuits
8. Staying Engaged with Modeling Of Electrical Overstress In Integrated Circuits
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Modeling Of Electrical Overstress In Integrated Circuits
9. Balancing eBooks and Physical Books Modeling Of Electrical Overstress In Integrated Circuits
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Modeling Of Electrical Overstress In Integrated Circuits
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Modeling Of Electrical Overstress In Integrated Circuits
 - Setting Reading Goals Modeling Of Electrical Overstress In Integrated Circuits
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Modeling Of Electrical Overstress In Integrated Circuits
 - Fact-Checking eBook Content of Modeling Of Electrical Overstress In Integrated Circuits
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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