

Coupled device, circuit and interconnect simulation

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Abstract:

In this paper, we discuss several aspects that are related to coupling device, circuit and interconnect simulation software. Straightforward co-simulation is too time-consuming, and hence reduced order modelling must be used in order to summarize the behaviour of individual simulations into compact models. From a theoretical point of view, the problem is complicated by the fact that equations of different type are being coupled. Mathematical techniques are indispensable for guaranteeing acceptable simulation times.

The European project CODESTAR aims at providing a framework in which the aforementioned coupled simulations can be performed. The examples given in this paper have been taken from that project.

1. Introduction

For the design of complex integrated systems, knowledge of the electromagnetic coupling in passive components like inductors, capacitors and critical parts of net lists are indispensable. Today's extraction software tools use the static approach to quantify this coupling, thereby ignoring the Maxwell or wave-dynamic aspect of electromagnetic radiation. Whereas such an approach is valid at moderate frequencies, high-frequency effects are a major design concern for the next generation of architectures. The International Technology Roadmap for Semiconductors recognizes the lack of appropriate future design tools. In particular design tools that include high frequency effects are a difficult challenge for a successful implementation of the 65 nm node corresponding to circuit frequencies exceeding 5 GHz. The effects are physically understood, but TCAD software programs that can deal with them are not available. Figure 1 (inspired by [6]) summarizes the effects that play a role in the analysis of passive structures: electric and magnetic coupling of segments through air and oxide, current crowding at edges due to the skin effect and eddy currents, proximity effects due to presence of nearby segments, radiation, substrate injection, and substrate current caused by ohmic, eddy and displacement currents.

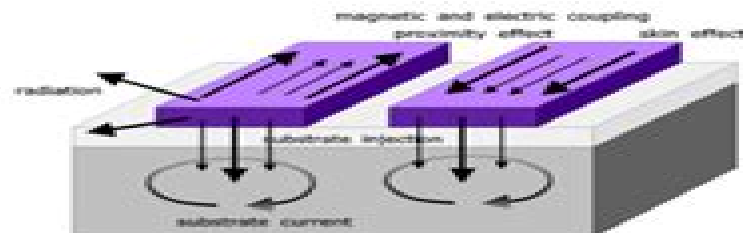


Figure 1. Summary of effects occurring in passive structures.

To accelerate the design of high-frequency passive on-chip structures and interconnects, the development of new modelling algorithms is needed. This task is addressed in the CODESTAR project. The resulting software will be used in a design cycle, starting from standardized geometrical data (GDS II format), and returning as output a manageable simulation net list that can be coupled to a network simulator such as SPICE or Pstar.

The situation becomes even more complicated when substrate noise analysis is required. As feature sizes decrease, substrate coupling noise may cause design failures and poor yields due to injected currents disturbing the operation of sensitive components. Any design targeted at sub-quarter micron process technologies may be vulnerable to substrate parasitics. Rule of thumb methodologies may turn out to be inadequate or lead to over-engineered designs. Reliable results can only be obtained by taking into account semiconductor physics. Tools like SubstrateStorm from Cadence perform such analyses by supplying RC net lists and reduced RC net lists, which can be coupled to network simulators. More accurate results are obtained when drift-diffusion models of semiconductor devices are used. In section 3 an example is given discussing precisely this topic, showing that it is indeed possible to couple device, circuit and interconnect simulations to obtain reliable models for substrate coupling noise.

Principles Of Circuit And Interconnect Simulation

O García

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Principles Of Circuit And Interconnect Simulation:

Circuit Simulation Principles and Techniques and Their Application Toward Interconnect Simulation Kirk Alan Ingemunson, 1994 Co-simulations of Microwave Circuits and High-Frequency Electromagnetic Fields Mei Song Tong, Xiao Yu Li, 2024-07-03 This book aims to provide many advanced application topics for microwave circuits and high frequency electromagnetic EM fields by using advanced design system ADS and high frequency structure simulator HFSS as simulation platforms In particular it contains the latest multidisciplinary co simulation guidance on the design of relevant components and devices Currently the circuit field design and performance analysis and optimization strongly rely on various kinds of robust electronic design automation EDA software RF microwave engineers must grasp two or more types of related simulation design software ADS by Keysight and HFSS by Ansys are the representative for circuit simulations and for field and structural simulations of microwave devices respectively At present these two types of software are widely used in enterprises universities and research institutions The main purpose of this book is to enable readers who are interested in microwave engineering and applied electromagnetics to master the applications of these two tools It also helps readers expand their knowledge boundaries behind those types of software and deepen their understanding of developing interdisciplinary technologies by co simulations The book is divided into three parts The first part introduces the two latest versions of ADS and HFSS and helps readers better understand the basic principles and latest functions better It also advises how to choose appropriate simulation tools for different problems The second part mainly describes co simulations for high frequency EM fields microwave circuits antenna designs EM compatibility EMC and thermal and structural analyses It provides guides and advices on performing co simulations by ADS and HFSS incorporated with other types of software respectively The last part narrates the automation interfaces and script programming methods for co simulations It primarily deals with the Advanced Extension Language AEL Python Data Link PDL and MATLAB interface in ADS For HFSS it discusses VBScript IronPython scripting and Application Programming Interface APIs based on MATLAB Each topic contains practical examples to help readers understand so that they can gain a solid knowledge and skills regarding automated interfaces and scripting methods based on these kinds of software Concisely written in combination with practical examples this book is very suitable as a textbook in introductory courses on microwave circuit and EM simulations and also as a supplementary textbook in many courses on electronics microwave engineering communication engineering and related fields As well it can serve as a reference book for microwave engineers and researchers *Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation* Rene van Leuken, Gilles Sicard, 2011-02-04 This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble France in September 2010 The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows circuit techniques low power circuits self timed

circuits process variation high level modeling of poweraware heterogeneous designs in SystemC AMS and minalogic

High-Speed Interconnects in VLSI Design, Modeling, and Signal Integrity Dr. Bhaskar Gugulothu, The rapid advancement in VLSI Very Large Scale Integration technology has ushered in a new era of high performance systems where interconnects have become a critical bottleneck in determining speed power and reliability This textbook provides a comprehensive understanding of high speed interconnect design analytical and simulation based modeling techniques and signal integrity challenges in modern integrated circuits It is intended for graduate students researchers and industry professionals involved in IC design and signal integrity analysis

Coupled Multiscale Simulation and Optimization in Nanoelectronics Michael Günther, 2015-06-15 Designing complex integrated circuits relies heavily on mathematical methods and calls for suitable simulation and optimization tools The current design approach involves simulations and optimizations in different physical domains device circuit thermal electromagnetic and in a range of electrical engineering disciplines logic timing power crosstalk signal integrity system functionality COMSON was a Marie Curie Research Training Network created to meet these new scientific and training challenges by a developing new descriptive models that take these mutual dependencies into account b combining these models with existing circuit descriptions in new simulation strategies and c developing new optimization techniques that will accommodate new designs The book presents the main project results in the fields of PDAE modeling and simulation model order reduction techniques and optimization based on merging the know how of three major European semiconductor companies with the combined expertise of university groups specialized in developing suitable mathematical models numerical schemes and e learning facilities In addition a common Demonstrator Platform for testing mathematical methods and approaches was created to assess whether they are capable of addressing the industry s problems and to educate young researchers by providing hands on experience with state of the art problems

Interconnects in VLSI Design Hartmut Grabinski, 2012-12-06 This book presents an updated selection of the most representative contributions to the 2nd and 3rd IEEE Workshops on Signal Propagation on Interconnects SPI which were held in Travemünde Baltic Sea Side Germany May 13 15 1998 and in Titisee Neustadt Black Forest Germany May 19 21 1999 This publication addresses the need of developers and researchers in the field of VLSI chip and package design It offers a survey of current problems regarding the influence of interconnect effects on the electrical performance of electronic circuits and suggests innovative solutions In this sense the present book represents a continuation and a supplement to the first book Signal Propagation on Interconnects Kluwer Academic Publishers 1998 The papers in this book cover a wide area of research directions Beneath the description of general trends they deal with the solution of signal integrity problems the modeling of interconnects parameter extraction using calculations and measurements and last but not least actual problems in the field of optical interconnects

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Johan Vounckx, Nadine Azemard, 2006-09-08 This book constitutes the refereed proceedings of the 16th International

Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more Analytical Methodology of Tree Microstrip Interconnects Modelling For Signal Distribution Blaise Ravelo, 2019-11-21 This book focuses on the modelling methodology of microstrip interconnects discussing various structures of single input multiple output SIMO tree interconnects for signal integrity SI engineering Further it describes lumped and distributed transmission line elements based on single input single output SIMO models of symmetric and asymmetric trees and investigates more complicated phenomenon such as interbranch coupling The modelling approaches are based on the analytical methods using the Z Y and T matrices The established method enables the S parameters and voltage transfer function of SIMO tree to be determined Providing illustrative results with frequency and time domain analyses for each tree interconnect structure the book is a valuable resource for researchers engineers and graduate students in fields of analogue RF microwave digital and mixed circuit design SI and manufacturing engineering

The 1984 Guide to the Evaluation of Educational Experiences in the Armed Services: Air Force American Council on Education, 1984

Proceedings of the Fourth International Symposium of Process Physics and Modeling in Semiconductor Technology G. R. Srinivasan, C. S. Murthy, Scott T. Dunham, 1996

Recent Topics on Modeling of Semiconductor Processes, Devices, and Circuits Rasit Onur Topaloglu, Peng Li, 2011 The last couple of years have been very busy for the semiconductor industry and researchers The rapid speed of production channel length reduction has brought lithographic challenges to semiconductor modeling These include stress optimization transisto

Model Reduction for Circuit Simulation Peter Benner, Michael Hinze, E. Jan W. ter Maten, 2011-03-25 Simulation based on mathematical models plays a major role in computer aided design of integrated circuits ICs Decreasing structure sizes increasing packing densities and driving frequencies require the use of refined mathematical models and to take into account secondary parasitic effects This leads to very high dimensional problems which nowadays require simulation times too large for the short time to market demands in industry Modern Model Order Reduction MOR techniques present a way out of this dilemma in providing surrogate models which keep the main characteristics of the device while requiring a significantly lower simulation time than the full model With Model Reduction for Circuit Simulation we survey the state of the art in the challenging research field of MOR for ICs and also address its future research directions Special emphasis is taken on aspects stemming from miniturisations to the nano scale Contributions cover complexity reduction using e g balanced truncation Krylov techniques or POD approaches For semiconductor applications a focus is on generalising current techniques to differential algebraic equations on including design parameters on preserving stability and on including nonlinearity by means of piecewise linearisations along solution trajectories TPWL and interpolation techniques for nonlinear

parts Furthermore the influence of interconnects and power grids on the physical properties of the device is considered and also top down system design approaches in which detailed block descriptions are combined with behavioral models Further topics consider MOR and the combination of approaches from optimisation and statistics and the inclusion of PDE models with emphasis on MOR for the resulting partial differential algebraic systems The methods which currently are being developed have also relevance in other application areas such as mechanical multibody systems and systems arising in chemistry and to biology The current number of books in the area of MOR for ICs is very limited so that this volume helps to fill a gap in providing the state of the art material and to stimulate further research in this area of MOR Model Reduction for Circuit Simulation also reflects and documents the vivid interaction between three active research projects in this area namely the EU Marie Curie Action ToK project O MOORE NICE members in Belgium The Netherlands and Germany the EU Marie Curie Action RTN project COMSON members in The Netherlands Italy Germany and Romania and the German federal project System reduction in nano electronics SyreNe Foundations for Microstrip Circuit Design Terry C.

Edwards, Michael B. Steer, 2016-02-01 Building on the success of the previous three editions Foundations for Microstrip Circuit Design offers extensive new updated and revised material based upon the latest research Strongly design oriented this fourth edition provides the reader with a fundamental understanding of this fast expanding field making it a definitive source for professional engineers and researchers and an indispensable reference for senior students in electronic engineering Topics new to this edition microwave substrates multilayer transmission line structures modern EM tools and techniques microstrip and planar transmission line design transmission line theory substrates for planar transmission lines Vias wirebonds 3D integrated interposer structures computer aided design microstrip and power dependent effects circuit models microwave network analysis microstrip passive elements and slotline design fundamentals **Circuit Analysis, Simulation and Design** Albert E. Ruehli, 1987 This book covers algorithmic aspects of computer aided circuit design for VLSI of large circuits The large scale aspect of VLSI requires a reorientation towards new and more efficient techniques Many algorithms have survived the test of time while others are suffering from the usual problem of polynomial or exponential running time complexity and storage requirements The approaches presented in this book are techniques which were developed in response to the VLSI problems The most recent exact circuit analysis and simulation techniques are presented such as waveform relaxation and timing simulation The book concentrates on the analysis and simulation of large circuits which exceed the capabilities of general purpose analyzers in both compute time and storage Also discussed are circuit models for switch level simulation techniques and circuit models for interconnections capacitance and inductances and optimization techniques The language and notation have been kept uniform throughout the book to help the reader to maintain the continuity between the topics discussed in the different chapters All algorithms are written in a Pascal style The terminology used should reflect the emerging language used in most of the VLSI circuit design community The book includes

proven approaches as well as techniques which are presently in a research state

Computer Principles and Design in Verilog HDL Yamin Li, Tsinghua University Press, 2015-08-17 Uses Verilog HDL to illustrate computer architecture and microprocessor design allowing readers to readily simulate and adjust the operation of each design and thus build industrially relevant skills Introduces the computer principles computer design and how to use Verilog HDL Hardware Description Language to implement the design Provides the skills for designing processor arithmetic cpu chips including the unique application of Verilog HDL material for CPU central processing unit implementation Despite the many books on Verilog and computer architecture and microprocessor design few if any use Verilog as a key tool in helping a student to understand these design techniques A companion website includes color figures Verilog HDL codes extra test benches not found in the book and PDFs of the figures and simulation waveforms for instructors

Bogatin's Practical Guide to Prototype Breadboard and PCB Design Eric Bogatin, 2021-09-30 Printed circuit boards PCB are at the heart of every electronic product manufactured today Yet engineers rarely learn to design PCBs from a class or course They learn it by doing by reading app notes watching YouTube videos and sitting by the side of an experienced engineer This book is the foundation building book for all engineers starting out to design PCBs It teaches good habits designing a PCB first for connectivity and secondly introduces the four most important principles to reduce noise A seven step process is presented developing a plan of record creating a Bill of Materials completing the schematic completing the layout completing the assembly conducting bring up and troubleshooting and documenting the project Each step is developed in detail In particular the emphasis in this book is on risk management what can be done at each step of the process to reduce the risk of a hard error which requires a complete re spin or a soft error which requires some sort of on the fly repair After connectivity is designed it s important to develop good habits to minimize the potential noise from ground bounce power rail stitching noise stack up design and reducing switching noise in signal paths These techniques apply to all designs from 2 layer to 8 layer and more for bandwidths below 200 MHz The best practices for manual lead free soldering are presented so that everyone can become a soldering expert The best measurement practices using common lab instruments such as the DMM the constant current constant voltage power supply and oscilloscopes are presented so that common artifacts are minimized Features in the design that help you find design or assembly errors quickly and the troubleshooting techniques to find and fix problems are introduced Applying the habits presented in this book will help every engineer design their next circuit board faster with less chance of an unexpected problem with the lowest noise This textbook will also have embedded videos to visually demonstrate many of the hands on processes introduced in this book

Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell

scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation José L. Ayala, Delong Shang, Alex Yakovlev, 2013-01-03 This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design PATMOS 2012 held in Newcastle UK Spain in September 2012 The 25 revised full papers presented were carefully reviewed and selected from numerous submissions The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems including reconfigurable hardware such as FPGAs The technical program focus on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization

Design and Crosstalk Analysis in Carbon Nanotube Interconnects P. Uma Sathyakam, Partha Sharathi Mallick, 2020-10-31 This book provides a single source reference on carbon nanotubes for interconnect applications It presents the recent advances in modelling and challenges of carbon nanotube CNT based VLSI interconnects Starting with a background of carbon nanotubes and interconnects this book details various aspects of CNT interconnect models the design metrics of CNT interconnects crosstalk analysis of recently proposed CNT interconnect structures and geometries Various topics covered include the use of semiconducting CNTs around metallic CNTs CNT

interconnects with air gaps use of emerging ultra low k materials and their integration with CNT interconnects and geometry based crosstalk reduction techniques This book will be useful for researchers and design engineers working on carbon nanotubes for interconnects for both 2D and 3D integrated circuits

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Nadine Azemard,Lars Svensson,2007-08-21 This volume features the refereed proceedings of the 17th International Workshop on Power and Timing Modeling Optimization and Simulation Papers cover high level design low power design techniques low power analog circuits statistical static timing analysis power modeling and optimization low power routing optimization security and asynchronous design low power applications modeling and optimization and more

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puréeing the soup with butter produces a rich silky texture

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