

Low Power CMOS VLSI Design: Implementation of Comparator Circuits Using Novel Technique

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Abstract -- Low power has emerged as a principal theme in today's electronic industry. Reduction of power consumption makes a device more reliable and efficient. As the demand of portable consumer electronics increases, and the size of the chip decreases, challenges towards the power dissipated are induced. Complementary Metal Oxide Semiconductor (CMOS) logic styles are best known for dissipating less energy or low power. The Proposed topology aims to design comparator logic circuits with different logic styles such as conventional CMOS, dynamic CMOS and domino CMOS. Initially, a single bit comparator will be designed and its functionality will be verified with all the three kinds of styles mentioned above. Using this design, by connecting them in a cascaded fashion, higher bit comparator circuits (4-bit and 8-bit) shall be obtained and a comparison will be drawn between the existing technology and the proposed design.

Keywords: CMOS logic, Comparators, Dynamic logic, dynamic CMOS, Low power

I. INTRODUCTION

A comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +ve VP, the input of the comparator is at a greater potential than the -ve VN, input, the output of the comparator is a logic 1, where as if the +ve input is at a potential less than the -ve input, the output of the comparator is at logic 0.

Figure 1. Comparator Operations.

If $V_P < V_N$ then $V_O = V_{SS} = \text{logic } 0$.
If $V_P > V_N$ then $V_O = V_{DD} = \text{logic } 1$.

II. LITERATURE REVIEW

According to Moore's Law, since the number of transistors integrated in a chip doubles once in every 18 months, thus, the role of circuit designers become very crucial. Decades ago, Speed and area were the important constraints and not power because the number of transistors involved in a design were quite less around

hundreds or thousands, but in the present scenario, as the complexity of the chips increase, millions of transistors are integrated in order to achieve the task with more functionalities and features. Hence, the power Dissipation of the overall chip or product is an extremely large value and has to be reduced significantly using suitable design techniques. This can be achieved by a number of ways such as reducing the number of transistors i.e. modifying the design which occupies a lesser number of transistors for the same functionality.

The main objective of this paper is to implement the higher bit comparator circuits with fewer transistors so that the total power dissipation will be reduced. We have implemented comparator circuits using conventional CMOS (Complementary Metal Oxide Semiconductor) and dynamic CMOS logic styles. Conventional CMOS technology implementation offers low power because of the nmos and pmos transistors behavior. While the pull

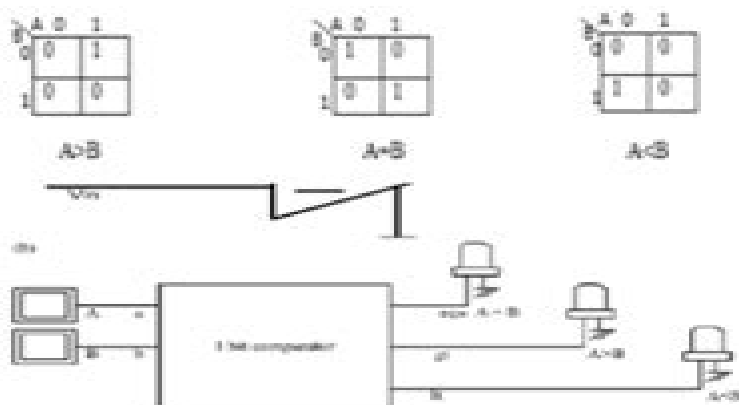


Figure 1.(a) Karnaugh map for a one – bit comparator.
Figure (b). Block diagram of a One – bit comparator.

up network is on, the pull down network is off and vice versa. So, the static power dissipation is ideally zero.

Low Power Cmos Design

**Anantha Chandrakasan, Robert W.
Brodersen**



Low Power Cmos Design:

Low-Power CMOS Design Anantha Chandrakasan, Robert W. Brodersen, 1998-02-11 This collection of important papers provides a comprehensive overview of low power system design from component technologies and circuits to architecture system design and CAD techniques LOW POWER CMOS DESIGN summarizes the key low power contributions through papers written by experts in this evolving field

Low Power Digital CMOS Design Anantha P. Chandrakasan, Robert W. Brodersen, 1995-06-30 Power consumption has become a major design consideration for battery operated portable systems as well as high performance desktop systems Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements A comprehensive approach is thus required at all levels of system design ranging from algorithms and architectures to the logic styles and the underlying technology Potentially one of the most important techniques involves combining architecture optimization with voltage scaling allowing a trade off between silicon area and low power operation Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology Several techniques can also be used to minimize the switched capacitance including representation optimizing signal correlations minimizing spurious transitions optimizing sequencing of operations activity driven power down etc The high efficiency of DC DC converter circuitry required for efficient low voltage and low current level operation is described by Stratakos Sullivan and Sanders The application of various low power techniques to a chip set for multimedia applications shows that orders of magnitude reduction in power consumption is possible The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design hierarchy Svensson of ISI describes emerging adiabatic switching techniques that can break the CV²f barrier and reduce the energy per computation at a fixed voltage Srivastava of AT T presents the application of aggressive shut down techniques to microprocessor applications

The Design and Implementation of Low-Power CMOS Radio Receivers Derek Shaeffer, Thomas H. Lee, 2007-05-08 It is hardly a profound observation to note that we remain in the midst of a wireless revolution In 1998 alone over 150 million cell phones were sold worldwide representing an astonishing 50% increase over the previous year Maintaining such a remarkable growth rate requires constant innovation to decrease cost while increasing performance and functionality Traditionally wireless products have depended on a mixture of semiconductor technologies spanning GaAs bipolar and BiCMOS just to name a few A question that has been hotly debated is whether CMOS could ever be suitable for RF applications However given the acknowledged inferiority of CMOS transistors relative to those in other candidate technologies it has been argued by many that CMOS RF is an oxymoron an endeavor best left cloistered in the ivory towers of academia In rebuttal there are several compelling reasons to consider CMOS for wireless applications Aside from the exponential device and density improvements delivered regularly by Moore's law only CMOS offers a technology path for integrating RF and digital elements potentially leading to exceptionally compact and low cost devices To enable this

achievement several thorny issues need to be resolved Among these are the problem of poor passive components broadband noise in MOSFETs and phase noise in oscillators made with CMOS Beyond the component level there is also the important question of whether there are different architectural choices that one would make if CMOS were used given the different constraints

Low-Power Cmos Vlsi Circuit Design Kaushik Roy, Sharat C. Prasad, 2009-02-02 This is the first book devoted to low power circuit design and its authors have been among the first to publish papers in this area Low Power CMOS VLSI Design Physics of Power Dissipation in CMOS FET Devices Power Estimation Synthesis for Low Power Design and Test of Low Voltage CMOS Circuits Low Power Static Ram Architectures Low Energy Computing Using Energy Recovery Techniques Software Design for Low Power

Low Power Design Methodologies Jan M. Rabaey, Massoud Pedram, 2012-12-06 Low Power Design Methodologies presents the first in depth coverage of all the layers of the design hierarchy ranging from the technology circuit logic and architectural levels up to the system layer The book gives insight into the mechanisms of power dissipation in digital circuits and presents state of the art approaches to power reduction Finally it introduces a global view of low power design methodologies and how these are being captured in the latest design automation environments The individual chapters are written by the leading researchers in the area drawn from both industry and academia Extensive references are included at the end of each chapter Audience A broad introduction for anyone interested in low power design Can also be used as a text book for an advanced graduate class A starting point for any aspiring researcher

Low Power Cmos Design Chandrakasan A., 2000-01-01 This is an essential reference for achieving longer battery lifetimes for portable devices details a broad range of practical techniques for reducing power dissipation in integrated circuits It provides an excellent background for new researchers and can serve as a comprehensive text book for graduate level courses

Low-Power CMOS Circuits Christian Piguet, 2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet's recently published *Low Power Electronics Design Low Power CMOS Circuits Technology Logic Design and CAD Tools* addresses the design of low power circuitry in deep submicron technologies It provides a focused reference for specialists involved in designing low power circuitry from transistors to logic gates The book is organized into three broad sections for convenient access The first examines the history of low power electronics along with a look at emerging and possible future technologies It also considers other technologies such as nanotechnologies and optical chips that may be useful in designing integrated circuits The second part explains the techniques used to reduce power consumption at low levels These include clock gating leakage reduction interconnecting and communication on chips and adiabatic circuits The final section discusses various CAD tools for designing low power circuits This section includes three chapters that demonstrate the tools and low power design issues at three major companies that produce logic synthesizers Providing detailed examinations contributed by leading experts

Low Power CMOS Circuits Technology Logic Design and CAD Tools supplies authoritative information on how to design and

model for high performance with low power consumption in modern integrated circuits It is a must read for anyone designing modern computers or embedded systems *Practical Low Power Digital VLSI Design* Gary K. Yeap, 2012-12-06 Practical Low Power Digital VLSI Design emphasizes the optimization and trade off techniques that involve power dissipation in the hope that the readers are better prepared the next time they are presented with a low power design problem The book highlights the basic principles methodologies and techniques that are common to most CMOS digital designs The advantages and disadvantages of a particular low power technique are discussed Besides the classical area performance trade off the impact to design cycle time complexity risk testability and reusability are discussed The wide impacts to all aspects of design are what make low power problems challenging and interesting Heavy emphasis is given to top down structured design style with occasional coverage in the semicustom design methodology The examples and design techniques cited have been known to be applied to production scale designs or laboratory settings The goal of Practical Low Power Digital VLSI Design is to permit the readers to practice the low power techniques using current generation design style and process technology Practical Low Power Digital VLSI Design considers a wide range of design abstraction levels spanning circuit logic architecture and system Substantial basic knowledge is provided for qualitative and quantitative analysis at the different design abstraction levels Low power techniques are presented at the circuit logic architecture and system levels Special techniques that are specific to some key areas of digital chip design are discussed as well as some of the low power techniques that are just appearing on the horizon Practical Low Power Digital VLSI Design will be of benefit to VLSI design engineers and students who have a fundamental knowledge of CMOS digital design **Low-Power CMOS Design for Wireless Transceivers** Alireza Zolfaghari, 2013-03-09 Low Power CMOS Design for Wireless Transceivers provides a comprehensive treatment of the challenges in low power RF CMOS design The author addresses trade offs and techniques that improve the performance from the component level to the architectural level Low Power CMOS Design for Wireless Transceivers deals with the design and implementation of low power wireless transceivers in a standard digital CMOS process This includes architecture circuits and monolithic passive components The book is written for engineers and graduate students interested in learning about wireless networks transceiver architectures stacked inductors design of RF front ends and the design of a 2.4 GHz transceiver **Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters** Vincenzo Peluso, Michiel Steyaert, Willy Sansen, 1999-02-28 Design of Low Voltage Low Power CMOS Delta Sigma A/D Converters investigates the feasibility of designing Delta Sigma Analog to Digital Converters for very low supply voltage lower than 1.5V and low power operation in standard CMOS processes The chosen technique of implementation is the Switched Opamp Technique which provides Switched Capacitor operation at low supply voltage without the need to apply voltage multipliers or low V_t MOST devices A method of implementing the classic single loop and cascaded Delta Sigma modulator topologies with half delay integrators is presented Those topologies are studied in order to find the parameters

that maximise the performance in terms of peak SNR Based on a linear model the performance degradations of higher order single loop and cascaded modulators compared to a hypothetical ideal modulator are quantified An overview of low voltage Switched Capacitor design techniques such as the use of voltage multipliers low V_t MOST devices and the Switched Opamp Technique is given An in depth discussion of the present status of the Switched Opamp Technique covers the single ended Original Switched Opamp Technique the Modified Switched Opamp Technique which allows lower supply voltage operation and differential implementation including common mode control techniques The restrictions imposed on the analog circuits by low supply voltage operation are investigated Several low voltage circuit building blocks some of which are new are discussed A new low voltage class AB OTA especially suited for differential Switched Opamp applications together with a common mode feedback amplifier and a comparator are presented and analyzed As part of a systematic top down design approach the non ideal charge transfer of the Switched Opamp integrator cell is modeled based upon several models of the main opamp non ideal characteristics Behavioral simulations carried out with these models yield the required opamp specifications that ensure that the intended performance is met in an implementation A power consumption analysis is performed The influence of all design parameters especially the low power supply voltage is highlighted Design guidelines towards low power operation are distilled Two implementations are presented together with measurement results The first one is a single ended implementation of a Delta Sigma ADC operating with 1.5V supply voltage and consuming 100 μ W for a 74 dB dynamic range in a 3.4 kHz bandwidth The second implementation is differential and operates with 900 mV It achieves 77 dB dynamic range in 16 kHz bandwidth and consumes 40 μ W

Design of Low Voltage Low Power CMOS Delta Sigma A/D Converters is essential reading for analog design engineers and researchers

Low-Power Electronics Design Christian Piguet, 2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today's methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now

Low Power VCO Design in CMOS Marc Tiebout, 2006-01-25 This work covers the design of CMOS fully integrated low power low phase noise voltage controlled

oscillators for telecommunication or datacommunication systems The need for low power is obvious as mobile wireless telecommunications are battery operated As wireless telecommunication systems use oscillators in frequency synthesizers for frequency translation the selectivity and signal to noise ratio of receivers and transmitters depend heavily on the low phase noise performance of the implemented oscillators Datacommunication systems need low jitter the time domain equivalent of low phase noise clocks for data detection and recovery The power consumption is less critical The need for multi band and multi mode systems pushes the high integration of telecommunication systems This is offered by sub micron CMOS featuring digital exibility The recent crisis in telecommunication clearly shows that mobile hand sets became mass market high volume consumer products where low cost is of prime importance This need for low cost products livens tremendously research towards CMOS alternatives for the bipolar or BiCMOS solutions in use today

Low Voltage, Low Power VLSI Subsystems
Kiat Seng Yeo, Kaushik Roy, 2005 Designers developing the low voltage low power chips that enable small portable devices face a very particular set of challenges This monograph details design techniques for the low power circuitry required by the many miniaturized business and consumer products driving the electronics market

Low-power HF Microelectronics
Gerson A. S. Machado, 1996 This book brings together innovative modelling simulation and design techniques in CMOS SOI GaAs and BJT to achieve successful high yield manufacture for low power high speed and reliable by design analogue and mixed mode integrated systems

Low-Power Digital VLSI Design Abdellatif Bellaouar, Mohamed I. Elmasry, 1995-06-30 A text that addresses the design of low power VLSI digital circuits and systems for senior undergraduate and graduate students and VLSI circuit and system designers working in industry It covers the basics from the process technologies and device modeling to the architecture It presents the fundamentals of power dissipation in CMOS circuits several practical circuit examples and low power techniques mainly in CMOS technology low voltage issues for digital CMOS and BiCMOS circuits advanced CMOS subsystem design and various power minimization techniques at the circuit logic architecture and algorithm level Annotation copyright by Book News Inc Portland OR

Low Power RF Circuit Design in Standard CMOS Technology
Unai Alvarado, Guillermo Bistu , I igo Ad n, 2011-10-18 Low Power Consumption is one of the critical issues in the performance of small battery powered handheld devices Mobile terminals feature an ever increasing number of wireless communication alternatives including GPS Bluetooth GSM 3G WiFi or DVB H Considering that the total power available for each terminal is limited by the relatively slow increase in battery performance expected in the near future the need for efficient circuits is now critical This book presents the basic techniques available to design low power RF CMOS analogue circuits It gives circuit designers a complete guide of alternatives to optimize power consumption and explains the application of these rules in the most common RF building blocks LNA mixers and PLLs It is set out using practical examples and offers a unique perspective as it targets designers working within the standard CMOS process and all the limitations inherent in these technologies

, **The Electrical Engineering Handbook** Wai Kai Chen, 2004-11-16 The Electrical

Engineer's Handbook is an invaluable reference source for all practicing electrical engineers and students. Encompassing 79 chapters, this book is intended to enlighten and refresh knowledge of the practicing engineer or to help educate engineering students. This text will most likely be the engineer's first choice in looking for a solution; extensive complete references to other sources are provided throughout. No other book has the breadth and depth of coverage available here. This is a must have for all practitioners and students. The Electrical Engineer's Handbook provides the most up to date information in Circuits and Networks, Electric Power Systems, Electronics, Computer Aided Design and Optimization, VLSI Systems, Signal Processing, Digital Systems and Computer Engineering, Digital Communication and Communication Networks, Electromagnetics and Control and Systems. About the Editor in Chief: Wai Kai Chen is Professor and Head Emeritus of the Department of Electrical Engineering and Computer Science at the University of Illinois at Chicago. He has extensive experience in education and industry and is very active professionally in the fields of circuits and systems. He was Editor in Chief of the IEEE Transactions on Circuits and Systems Series I and II, President of the IEEE Circuits and Systems Society and is the Founding Editor and Editor in Chief of the Journal of Circuits, Systems and Computers. He is the recipient of the Golden Jubilee Medal, the Education Award and the Meritorious Service Award from the IEEE Circuits and Systems Society and the Third Millennium Medal from the IEEE. Professor Chen is a fellow of the IEEE and the American Association for the Advancement of Science. 77 chapters encompass the entire field of electrical engineering. THOUSANDS of valuable figures, tables, formulas and definitions. Extensive bibliographic references.

Low-Power VLSI Circuits and Systems Ajit Pal, 2014-11-17. The book provides a comprehensive coverage of different aspects of low power circuit synthesis at various levels of design hierarchy starting from the layout level to the system level. For a seamless understanding of the subject, basics of MOS circuits have been introduced at transistor, gate and circuit level, followed by various low power design methodologies such as supply voltage scaling, switched capacitance minimization techniques and leakage power minimization approaches. The content of this book will prove useful to students, researchers as well as practicing engineers.

Power Aware Design Methodologies Massoud Pedram, Jan M. Rabaey, 2007-05-08. Power Aware Design Methodologies was conceived as an effort to bring all aspects of power aware design methodologies together in a single document. It covers several layers of the design hierarchy from technology, circuit, logic and architectural levels up to the system layer. It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits, digital and analog systems on chip, microelectronic systems, wirelessly networked systems of computational nodes and so on. In addition to providing an in depth analysis of the sources of power dissipation in VLSI circuits and systems and the technology and design trends, this book provides a myriad of state of the art approaches to power optimization and control. The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas. Contributions are from both academia and industry. The contributors have reported the various technologies, methodologies and techniques in such a

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