

Performance Analysis of 3D Stacked Memory Architectures in High Performance Computing

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Abstract: The increasing speed of the CPU is greater than that of the RAM. The 'Memory Wall' issue, which occurs when the processor runs out of data, could occur. The I/O infrastructure is strained as the number of cores in CMPs rises because more data is needed from the memory subsystem. Memory bandwidth becomes a bottleneck in terms of performance. By layering memories on top of logic, three-dimensional integrated circuits are proposed as a solution to this problem. The widely-used compute-in-memory benchmark framework 'NeuroSim' is utilized by us to investigate the benefits of a three-dimensional design for a Neural Network application.

Keywords: 3D Stacked Memory, Compute in Memory, Monolithic 3D Integration, Neural Networks

I. INTRODUCTION

Most computer chores are done by the processor (CPU) getting data and instructions from main memory, which is usually an external memory that uses DRAMs, and then running them in order. Processors are becoming more and more efficient at a rate of about 60% per year thanks to new methods and technologies being used. On the other hand, DRAM technology and access times have been getting better at a rate of less than 10% per year. When more data needs to be retrieved from memory, the I/O system has to work harder to make sure there is enough memory speed. This type of 2D integrated circuit has the main memory and processor on two different chips. Because the bus link between chips is so long, there are a lot of capacitive loads. This makes the process of moving data from main memory to the CPU very slow and uses a lot of power. Because logic and memory don't work together as well as they should, microprocessor makers have had to come up with complicated, energy-hungry architectures that allow for out-of-order and speculative execution. To hide the delay in main memory, computers have also been made with bigger and bigger cache hierarchies. People often call these kinds of problems "Memory Wall problems." Applications that use a lot of data, like machine learning, neural network calculations, and real-time data analytics, are directly affected by the memory wall limit.

One way to deal with this problem is to bring the main memory closer to the processor die thus reducing access latencies, by using 2.5D or 3D packaging. In a 2.5D structure, the processor and memory are placed side-by-side on a silicon interposer to achieve extremely high die-to-die

interconnect density. In a 3D stacked structure, DRAM memory is stacked on top of the logic layer, bonded with vertical interconnects.

3D stacking enables an increase in bandwidth by using these dense interconnects instead of traditional I/O pins, allows for mixing dissimilar process technologies such as high-speed CMOS with high-density DRAM leading to an increase in on-chip memory capacity, as well as reductions in power requirements by reducing the number of external I/O drivers and interconnects [1].

Some issues with building in the third dimension, in the integration of different process technologies (and materials) together can be challenging. Further, reliability issues can be induced due to stress from higher tiered layers in the stack. Additionally, power dissipation has major influence as the high-power compute layers can create thermal hotspots in the stacked memory modules, especially those near the centre which are far away from the heat sink.

II. BACKGROUND STUDY

G. H. Loh [2] examines the integration of 3D DRAM in multicore computers, with the control and peripheral access circuitry being located on a distinct CMOS technology layer specifically designated for this purpose. The test cells are fabricated using vertically stacked NMOS technology, with Through-Silicon Vias employed for interconnecting the layers. This design implements a distributed architecture for DRAM ranks, utilising multiple layers instead of a single layer. This results in a 32% reduction in memory access time for a DRAM with five layers. The authors propose the utilisation of a vector bloom filter to enhance the functionality of the L2 miss handling architecture (MHA) in order to optimise the additional capacity provided by the 3D-stacked memory system. The test findings indicate that the proposed method of memory organisation is 1.75 times more efficient than alternative 3D DRAM concepts when performing memory-intensive jobs on a quad-core CPU.

D. H. Woo et al. [3] suggest a 3D-stacked memory architecture with a vertical L2 network using a large array of high-density TSVs to improve memory bandwidth even further. Their results show at least a 1.27x speedup over traditional 3D stacked DRAM architectures.

D. Lee et al. [4] explore another approach to better utilize the total potential bandwidth increase offered by TSVs for 3D stacked DRAMs. Their proposed architecture delivers an

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Igor Tartalja, Veljko Milutinović



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Durable Phase-Change Memory Architectures, 2020-02-24 Advances in Computers Volume 118 the latest volume in this innovative series published since 1960 presents detailed coverage of new advancements in computer hardware software theory design and applications Chapters in this updated release include Introduction to non volatile memory technologies The emerging phase change memory Phase change memory architectures Inter line level schemes for handling hard errors in PCMs Handling hard errors in PCMs by using intra line level schemes and Addressing issues with MLC Phase change Memory Algorithms and Architectures for Parallel Processing Guojun Wang,Albert Zomaya,Gregorio Martinez,Kenli Li,2015-11-16 This four volume set LNCS 9528 9529 9530 and 9531 constitutes the refereed proceedings of the 15th International Conference on Algorithms and Architectures for Parallel Processing ICA3PP 2015 held in Zhangjiajie China in November 2015 The 219 revised full papers presented together with 77 workshop papers in these four volumes were carefully reviewed and selected from 807 submissions 602 full papers and 205 workshop papers The first volume comprises the following topics parallel and distributed architectures distributed and network based computing and internet of things and cyber physical social computing The second volume comprises topics such as big data and its applications and parallel and distributed algorithms The topics of the third volume are applications of parallel and distributed computing and service dependability and security in distributed and parallel systems The covered topics of the fourth volume are software systems and programming models and performance modeling and evaluation **Quality of Service Architectures for Wireless Networks: Performance Metrics and Management** Adibi, Sasan,Jain, Raj,Parekh, Shyam,Tofiqbakhsh, Mostafa,2010-01-31 This book further explores various issues and proposed solutions for the provision of Quality of Service QoS on the wireless networks Provided by publisher Algorithms and Architectures for Parallel Processing, Part I Yang Xiang,Alfredo Cuzzocrea,Michael Hobbs,Wanlei Zhou,2011-10-07 This two volume set LNCS 7016 and LNCS 7017 constitutes the refereed proceedings of the 11th International Conference on Algorithms and Architectures for Parallel Processing ICA3PP 2011 held in Melbourne Australia in October 2011 The first volume presents 24 revised regular papers and 17 revised short papers together with the abstract of the keynote lecture all carefully reviewed and selected from 85 initial submissions The papers cover the many dimensions of parallel algorithms and architectures encompassing fundamental theoretical approaches practical experimental results and commercial components and systems and focus on two broad areas of parallel and distributed computing i e architectures algorithms and networks and systems and applications *Micro Electronic Circuit Design for High Performance Applications* Dr. S.Sathya,Dr. Priyanka Veeramosu,Dr. R. Boopathi,Dr. Bindu K V,Mr. Nishant S,2025-01-28 Microelectronic Circuit Design for High Performance Applications is a comprehensive that explores advanced circuit design principles tailored for high speed low power and efficient electronic systems Topics such as semiconductor devices analog and digital circuit design signal integrity and power management the

book provides in depth insights into optimizing performance in modern electronic applications It integrates theoretical foundations with practical design methodologies making it valuable for engineers researchers and students involved in cutting edge microelectronics With a focus on emerging technologies the addresses challenges in miniaturization integration and high frequency operation ensuring relevance in contemporary and future electronic design

Redis Mastery: Advanced Techniques for Scalable Data Architecture Adam Jones, 2025-01-03 Unleash the full potential of your data with Redis Mastery Advanced Techniques for Scalable Data Architecture the ultimate guide to mastering Redis an essential in memory database that amplifies application performance This comprehensive tome takes you beyond the basics delving into sophisticated techniques that propel your data architecture to new heights Explore the intricacies of Redis s robust data structures secure and fine tune your deployment and tackle advanced challenges like seamless scaling and ensuring high availability Discover diverse applications from powering real time analytics to managing complex message queues Whether you re a developer seeking to optimize application efficiency a system administrator focused on resilient data stores or a tech enthusiast eager to master cutting edge database solutions this book is your indispensable resource With lucid explanations practical demonstrations and seasoned advice Redis Mastery equips you to harness Redis s full capabilities Revolutionize your data handling with advanced techniques that augment durability and enable effortless scalability Elevate your data strategy and build high performance future ready applications with Redis Mastery Advanced Techniques for Scalable Data Architecture Redis is your gateway to crafting applications that excel under pressure and adapt seamlessly to ever evolving demands Secure your copy today and embark on your journey to becoming a Redis virtuoso

Guide to Test Automation

Architecture Craig Risi, 2025-08-26 DESCRIPTION In the software development domain test automation has emerged as the cornerstone of delivering reliable applications This comprehensive guide provides a systematic roadmap for designing and implementing test automation frameworks that transcend tool specific limitations ensuring they adapt and endure You will learn to apply core software architectural principles including modularity loose coupling and layering to your test code The book offers practical guidance on managing test data orchestrating parallel test executions and integrating seamlessly with CI CD pipelines using quality gates Furthermore it details how to expand your framework s capabilities to include non functional testing such as security performance and resilience Through detailed case studies you will gain a clear understanding of what it takes to build a scalable framework from scratch migrate a legacy system and foster continuous architectural improvement With insights into emerging trends like AI driven automation and predictive analytics this book is both a toolkit and a strategic guide It empowers architects testers and developers alike to embrace complexity and lead the way in modern test automation

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pipelines Handling modern testing challenges Leverage AI ML to create self healing and predictive test suites WHO THIS BOOK IS FOR This book is for software architects SDETs software engineers and quality engineers responsible for designing and developing test automation frameworks Readers should have a foundational understanding of programming concepts and software development lifecycle principles before diving in TABLE OF CONTENTS Prologue 1 Introduction to Test Automation 2 Understanding Test Automation Frameworks 3 Designing with Architecture in Mind 4 Designing Modular Test Frameworks 5 Testability and Software Design 6 Test Orchestration and Execution 7 Test Data Management 8 CI CD Integration and Quality Gates 9 Handling Asynchronous and Distributed Systems 10 Security Performance and Resilience Testing 11 Overview of Tools Used in Test Automation 12 Case Study Building a Scalable Framework From Scratch 13 Case Study Migrating to a Tool agnostic Framework 14 Case Study Framework Evolution and Continuous Improvement 15 Embracing AI and ML in Test Automation 16 Emerging Trends and Technologies 17 Conclusion The Path to Sustainable Test Automation Frameworks Appendix Glossary of Terms

OpenCL Programming and Architecture Richard Johnson, 2025-06-03 OpenCL Programming and Architecture OpenCL Programming and Architecture is a comprehensive guide that delves into the principles models and advanced concepts of parallel computing with OpenCL Starting with the historical evolution of heterogeneous computing and the foundational design goals of the OpenCL standard this book thoroughly explains the platform s architectural abstractions and execution models Readers are guided through essential topics such as the memory hierarchy device types and capabilities enabling a deep understanding of how OpenCL unifies programming across CPUs GPUs FPGAs and other accelerators The book offers a meticulous exploration of the OpenCL programming model including the kernel language specification kernel development NDRange organization and synchronization mechanisms Practical memory management techniques are discussed in depth from buffer and image object handling to efficient data transfers and advanced address space management Further chapters examine device and platform interoperability helping developers navigate multi device programming graphics API integration workload scheduling and portability across diverse architectures all crucial for building robust scalable and high performance parallel applications Rounding out the coverage OpenCL Programming and Architecture presents invaluable guidance on profiling tuning and optimizing OpenCL applications as well as advanced parallel programming patterns such as reductions stencils and asynchronous execution The final chapters focus on debugging testing and ensuring reliability followed by an examination of emerging topics like SPIR V machine learning accelerators and security in OpenCL Complete with real world case studies and best practices this book is an indispensable resource for system programmers software engineers and researchers striving to harness the power of heterogeneous computing with OpenCL

High Performance Embedded Architectures and Compilers André Seznec, Michael O'Boyle, Joel Emer, Margaret Martonosi, Theo Ungerer, 2009-01-12 This book constitutes the refereed proceedings of the Fourth International Conference on High Performance Embedded Architectures and Compilers

HiPEAC 2009 held in Paphos Cyprus in January 2009 The 27 revised full papers presented together with 2 invited keynote paper were carefully reviewed and selected from 97 submissions The papers are organized in topical sections on dynamic translation and optimisation low level scheduling parallelism and resource control communication mapping for CMPs power cache issues as well as parallel embedded applications **Computational Fluid Dynamics and Heat Transfer** Ryoichi Amano,Bengt Sundén,2011 Heat transfer and fluid flow issues are of great significance and this state of the art edited book with reference to new and innovative numerical methods will make a contribution for researchers in academia and research organizations as well as industrial scientists and college students The book provides comprehensive chapters on research and developments in emerging topics in computational methods e g the finite volume method finite element method as well as turbulent flow computational methods Fundamentals of the numerical methods comparison of various higher order schemes for convection diffusion terms turbulence modeling the pressure velocity coupling mesh generation and the handling of arbitrary geometries are presented Results from engineering applications are provided Chapters have been co authored by eminent researchers **Advanced Computer Architecture** Junjie Wu,Haibo Chen,Xingwei Wang,2014-07-21 This book constitutes the refereed proceedings of the 10th Annual Conference on Advanced Computer Architecture ACA 2014 held in Shenyang China in August 2014 The 19 revised full papers presented were carefully reviewed and selected from 115 submissions The papers are organized in topical sections on processors and circuits high performance computing GPUs and accelerators cloud and data centers energy and reliability intelligence computing and mobile computing **Algorithms and Architectures for Parallel Processing** Yang Xiang,Ivan Stojmenovic,Bernady O. Apduhan,Guojun Wang,Koji Nakano,Albert Y. Zomaya,2012-09-04 The two volume set LNCS 7439 and 7440 comprises the proceedings of the 12th International Conference on Algorithms and Architectures for Parallel Processing ICA3PP 2012 as well as some workshop papers of the CDCN 2012 workshop which was held in conjunction with this conference The 40 regular paper and 26 short papers included in these proceedings were carefully reviewed and selected from 156 submissions The CDCN workshop attracted a total of 19 original submissions 8 of which are included in part II of these proceedings The papers cover many dimensions of parallel algorithms and architectures encompassing fundamental theoretical approaches practical experimental results and commercial components and systems **Die-stacking Architecture** Yuan Xie,Jishen Zhao,2022-05-31 The emerging three dimensional 3D chip architectures with their intrinsic capability of reducing the wire length promise attractive solutions to reduce the delay of interconnects in future microprocessors 3D memory stacking enables much higher memory bandwidth for future chip multiprocessor design mitigating the memory wall problem In addition heterogenous integration enabled by 3D technology can also result in innovative designs for future microprocessors This book first provides a brief introduction to this emerging technology and then presents a variety of approaches to designing future 3D microprocessor systems by leveraging the benefits of low latency high bandwidth and heterogeneous

integration capability which are offered by 3D technology Computer Organisation and Architecture Author: Dr.Kapil Chaudhary Dr.Kapil Chaudhary,2025-10-15 It s with great happiness that I would like to acknowledge a great deal of people that get helped me extremely through the entire difficult challenging but a rewarding and interesting path towards some sort of Edited Book without having their help and support none of this work could have been possible **Architecture of Computing Systems - ARCS 2018** Mladen Berekovic,Rainer Buchty,Heiko Hamann,Dirk Koch,Thilo Pionteck,2018-04-05 This book constitutes the proceedings of the 31st International Conference on Architecture of Computing Systems ARCS 2018 held in Braunschweig Germany in April 2018 The 23 full papers presented in this volume were carefully reviewed and selected from 53 submissions ARCS has always been a conference attracting leading edge research outcomes in Computer Architecture and Operating Systems including a wide spectrum of topics ranging from embedded and real time systems all the way to large scale and parallel systems **NVMe Architecture and Protocols** Richard Johnson,2025-06-01 NVMe Architecture and Protocols NVMe Architecture and Protocols offers a comprehensive exploration of Non Volatile Memory Express NVMe technologies tailored for engineers architects and technical professionals navigating the rapidly evolving landscape of high performance storage Beginning with the foundations of NVMe s inception the book meticulously charts the evolution from legacy protocols to NVMe s revolutionary approach detailing the motivations design philosophies and ecosystem transformations that have positioned NVMe as the protocol of choice for modern data intensive applications Through clear comparisons targeted use cases and insights into new feature developments readers gain a thorough understanding of NVMe s transformative impact on storage efficiency and scalability Delving deeper the book demystifies the interplay between hardware and system architecture unpacking topics such as PCI Express integration queuing strategies memory access mechanisms and power management Comprehensive chapters address the full breadth of NVMe protocol fundamentals including command models submission and completion queue management asynchronous event handling and robust error recovery Advanced sections illuminate extensions like Zoned Namespaces key value stores end to end data protection and persistent memory support as well as the groundbreaking expansion of NVMe over Fabrics NVMe oF which brings high speed NVMe capabilities to distributed and cloud environments through protocols like RDMA TCP and Fibre Channel The book s holistic approach extends to the software stack and operational realities from device drivers and firmware to virtualization and performance tuning Critical themes of security reliability and data integrity are addressed in concert with quality of service and fault tolerance providing actionable guidance for deploying monitoring and securing NVMe in production environments Looking toward the future NVMe Architecture and Protocols evaluates next generation standards integration with emerging memory technologies and the protocol s adaptation for AI edge IoT and composable infrastructure making this an indispensable resource for those building the next generation of storage solutions High Performance Embedded Architectures and Compilers Per Stenström,Michel Dubois,Manolis Katevenis,Rajiv Gupta,Theo

Ungerer,2008-01-18 This highly relevant and up to the minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2008 held in G teborg Sweden January 27 29 2008 The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions The papers are organized into topical sections on a number of key subjects in the field

Proceedings of the 1993 International Conference on Parallel Processing C.Y. Roger Chen,P. Bruce Berra,1993-08-16 This three volume work presents a compendium of current and seminal papers on parallel distributed processing offered at the 22nd International Conference on Parallel Processing held August 16 20 1993 in Chicago Illinois Topics include processor architectures mapping algorithms to parallel systems performance evaluations fault diagnosis recovery and tolerance cube networks portable software synchronization compilers hypercube computing and image processing and graphics Computer professionals in parallel processing distributed systems and software engineering will find this book essential to their complete computer reference library

Embedded Computer Systems: Architectures, Modeling, and Simulation Luigi Carro,Francesco Regazzoni,Christian Pilato,2025-01-27 The two volume set LNCS 15226 and 15227 constitutes the refereed proceedings of the 24th International Conference on Embedded Computer Systems Architectures Modeling and Simulation SAMOS 2024 held in Samos Greece during June 29 July 4 2024 The 24 full papers 10 full papers in 2 special sessions and 4 poster session included in this book were carefully reviewed and selected from 57 submissions This SAMOS 2024 covers the topics systems themselves through their applications architectures and underlying processors or methods created to automate their design

The Cache Coherence Problem in Shared-Memory Multiprocessors Igor Tartalja,Veljko Milutinović,1996-02-13 Almost all software solutions are developed through academic research and implemented only in prototype machines leaving the field of software techniques for maintaining the cache coherence widely open for future research and development This book is a collection of all the representative approaches to software coherence maintenance including a number of related efforts in the performance evaluation field The book presents a selection of 27 papers dealing with state of the art software solutions for cache coherence maintenance in shared memory multiprocessors It begins with a set of four introductory readings that provides a brief overview of the cache coherence problem and introduces software solutions to the problem The text defines and illustrates static and dynamic software schemes techniques for modeling performance evaluation mechanisms and performance evaluation studies The book is intended for the experienced reader in computer engineering but possibly a novice in the topic of cache coherence It also provides an in depth understanding of the problem as well as a comprehensive overview for multicomputer designers computer architects and compiler writers In addition it is a software coherence reference handbook for advanced undergraduate and typical graduate students in multiprocessing and multiprogramming areas

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