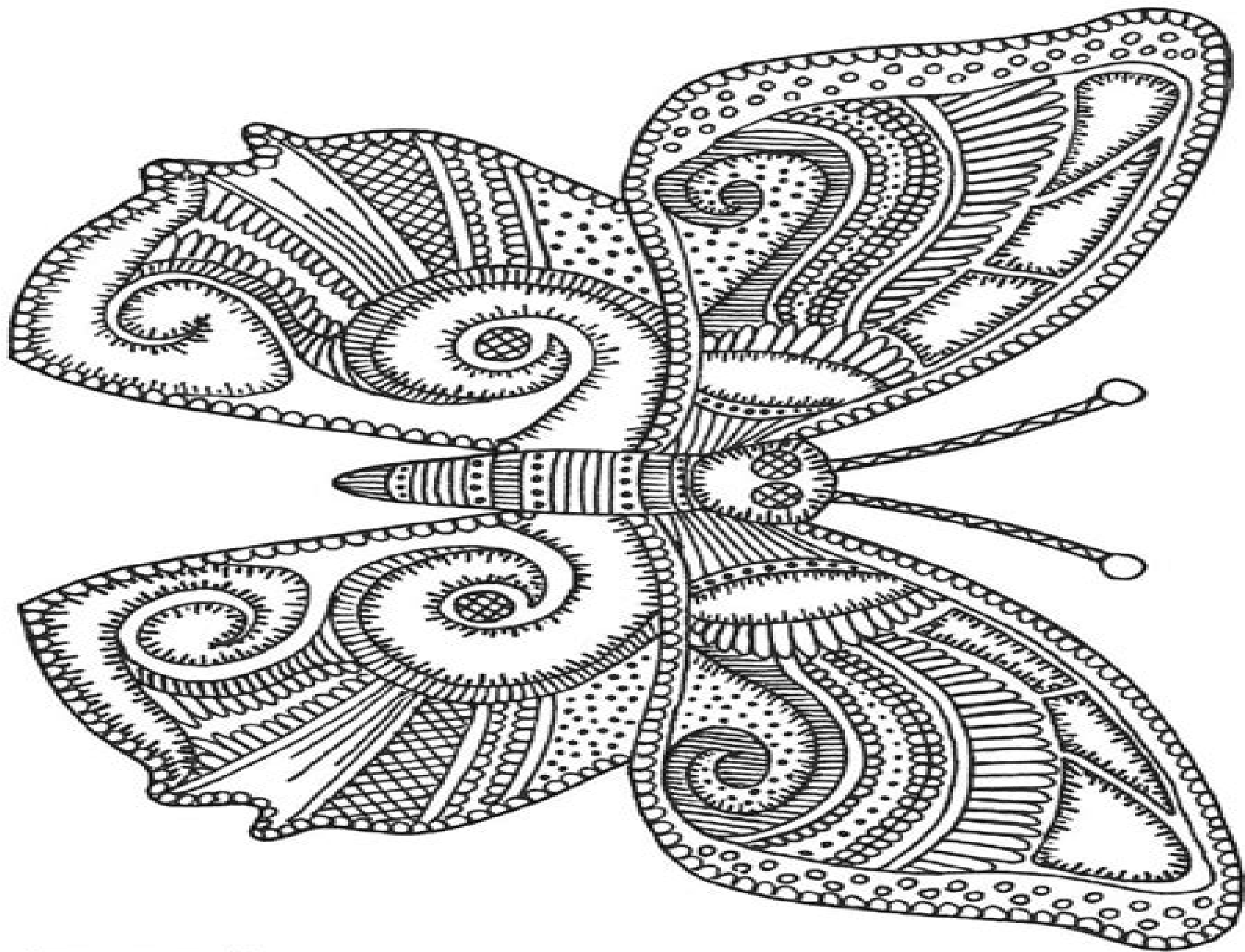




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Jin-Ying Zhang



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wire enable input wire 7 0 a input wire 7 0 b output wire 15 0 c