

Cs FREQUENCY SYNTHESIS: A NEW APPROACH

A. Sen Gupta⁺, D. Popović[#], and F. L. Walls^{*}⁺National Physical Laboratory, New Delhi, India[#]University of Belgrade, Belgrade, Yugoslavia^{*}National Institute of Standards and Technology, Boulder CO, USA

ABSTRACT

This paper describes a new approach to synthesizing the Cs hyperfine frequency of 9.192 GHz that is designed to be sufficiently rugged for use in space, specifically for the primary atomic reference clock in space (PARCS) planned for the international space station, as well as ground applications. This new approach requires no narrow band filters or frequency multiplication and the primary source of cooling is conduction. Instead of frequency multiplication, it uses a custom regenerative divider stage followed by two commercial binary dividers and several mixing stages. A fractional frequency step of 2×10^{-14} is achieved by mixing the output of a 48 bit numerically controlled oscillator with the microwave signal. Preliminary tests on the new synthesizer design indicate an internal fractional frequency stability of 1×10^{-13} at 10 s and 1×10^{-14} at 1 day, dominated by the daily room temperature variations. The phase and amplitude noise are similar to our previous designs that used frequency multiplication and narrow band filters. The temperature coefficient is less than $0.2 \text{ ps/}^\circ\text{C}$.

1. INTRODUCTION

Within the last decade new generations of frequency standards based on laser cooled atoms and ions with stabilities approaching 10^{-16} at 1 day have been developed [1-3]. At these stabilities, the performance of the local oscillator and the microwave synthesis chain appear to be limiting factors. To support NIST's new standards, we have designed a new generation of microwave frequency synthesizers [4-6]. The basic criteria for these designs have been high resolution, low phase modulation (PM) and amplitude modulation (AM) noise, low spurs near the carrier, and very high phase stability with respect to environmental effects.

The aim of the present work was to design a microwave synthesizer for a laser cooled Cs fountain compatible for use in space, specifically for a slow beam Cs primary atomic reference clock in space (PARCS) scheduled for flight the international space

station [7]. This required the use of components that are or can be space-qualified. Other major design goals were that the synthesizer be compact, robust, consume low power, and very importantly, that all dissipated heat be removed by conduction and radiation as there is minimal convection in space. The performance goal was a frequency resolution of at least 10^{-13} and a fractional frequency stability at 1 day of lower than 1×10^{-14} .

In the following section we describe our design. The approach yields a simple synthesis scheme that avoids frequency multiplication, narrow band filters, and phase-locked loops while still producing an output that is suitable with high resolution. We also discuss some initial performance results of the two units that were constructed. All performance goals were met or exceeded.

2. DESIGN DETAILS

Figure 1 shows a schematic block diagram of the synthesizer. The output of a 6.4 GHz voltage-controlled dielectric resonant oscillator (DRO) drives a custom regenerative divide-by-2 circuit [8], comprised of a mixer, a 3.2 GHz low-pass filter, and an amplifier in a closed-loop configuration. This regenerative divider provides low PM noise [9], a very low coefficient of phase shift with temperature, and simultaneous outputs at 0.5 and 1.5 times the input frequency, i.e., at 3.2 GHz and 9.6 GHz. The 3.2 GHz and 9.6 GHz outputs are separated using a diplexer.

The 3.2 GHz output is divided to 100 MHz using a commercial divide-by-8 followed by a commercial divide-by-4 [10]. The 100 MHz output of the dividers is low-pass filtered and buffered in a two-stage amplifier to provide the output reference frequency.

Another key constituent of the synthesizer is a numerically controlled oscillator using a direct digital synthesis (DDS) chip with 48 bit resolution [11]. This unit is clocked by a 50 MHz signal obtained by dividing the 100 MHz by 2. This DDS chip not only provides the high resolution and low spurs, but it is also available in a space-qualified version. The DDS output is a sine wave, which can be set to a resolution of 0.2 μHz and a rate up to 20 MHz using 14 data and control lines. Another feature of this DDS is that its frequency

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