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Low Dielectric Constant Materials for IC Applications



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the senior college level Highlighting emerging organic and polymeric optoelectronic materials and devices it presents the fundamentals principle mechanisms representative examples and key data

Synthesis and Applications in Microelectronics Toh-Ming Lu,1995 **Low-dielectric Constant Materials--**

Metal-Dielectric Interfaces in Gigascale Electronics Ming He,Toh-Ming Lu,2012-02-02 Metal dielectric interfaces are ubiquitous in modern electronics As advanced gigascale electronic devices continue to shrink the stability of these interfaces is becoming an increasingly important issue that has a profound impact on the operational reliability of these devices In this book the authors present the basic science underlying the thermal and electrical stability of metal dielectric interfaces and its relationship to the operation of advanced interconnect systems in gigascale electronics Interface phenomena including chemical reactions between metals and dielectrics metallic atom diffusion and ion drift are discussed based on fundamental physical and chemical principles Schematic diagrams are provided throughout the book to illustrate interface phenomena and the principles that govern them Metal Dielectric Interfaces in Gigascale Electronics provides a unifying approach to the diverse and sometimes contradictory test results that are reported in the literature on metal dielectric interfaces The goal is to provide readers with a clear account of the relationship between interface science and its applications in interconnect structures The material presented here will also be of interest to those engaged in field effect transistor and memristor device research as well as university researchers and industrial scientists working in the areas of electronic materials processing semiconductor manufacturing memory chips and IC design

Smart Power ICs Bruno Murari,2002-06-13 This book provides a survey of the state of the art of technology and future trends in the new family of Smart Power ICs and describes design and applications in a variety of fields ranging from automotive to telecommunications reliability evaluation and qualification procedures The book is a valuable source of information and reference for both power IC design specialists and to all those concerned with applications the development of digital circuits and with system architecture

Copper Interconnect Technology Tapan Gupta,2010-01-22 Since overall circuit performance has depended primarily on transistor properties previous efforts to enhance circuit and system speed were focused on transistors as well During the last decade however the parasitic resistance capacitance and inductance associated with interconnections began to influence circuit performance and will be the primary factors in the evolution of nanoscale ULSI technology Because metallic conductivity and resistance to electromigration of bulk copper Cu are better than aluminum use of copper and low k materials is now prevalent in the international microelectronics industry As the feature size of the Cu lines forming interconnects is scaled resistivity of the lines increases At the same time electromigration and stress induced voids due to increased current density become significant reliability issues Although copper low k technology has become fairly mature there is no single book available on the promise and challenges of these next generation technologies In this book a leader in the field describes advanced laser systems with lower radiation wavelengths photolithography materials and mathematical modeling approaches

to address the challenges of Cu interconnect technology *Power Management of Digital Circuits in Deep Sub-Micron CMOS Technologies* Stephan Henzler, 2006-11-24 In the deep sub micron regime the power consumption has become one of the most important issues for competitive design of digital circuits Due to dramatically increasing leakage currents the power consumption does not take advantage of technology scaling as before State of art power reduction techniques like the use of multiple supply and threshold voltages transistor stack forcing and power gating are discussed with respect to implementation and power saving capability Focus is given especially on technology dependencies process variations and technology scaling Design and implementation issues are discussed with respect to the trade off between power reduction performance degradation and system level constraints A complete top down design flow is demonstrated for power gating techniques introducing new design methodologies for the switch sizing task and circuit blocks for data retention and block activation The leakage reduction ratio and the minimum power down time are introduced as figures of merit to describe the power gating technique on system level and give a relation to physical circuit parameters Power Management of Digital Circuits in Deep Sub Micron CMOS Technologies mainly deals with circuit design but also addresses the interface between circuit and system level design on the one side and between circuit and physical design on the other side

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