## Regular Fabrics in Deep Sub-Micron Integrated-Circuit Design

Fan Mo and Robert K. Brayton

# Regular Fabrics In Deep Submicron Integratedcircuit Design

Sudeep Pasricha, Nikil Dutt

#### Regular Fabrics In Deep Submicron Integrated circuit Design:

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be used for on chip communication design The design issues are handled on physical and circuit layer logic and architecture layer and from system design methodology and tools point of view Formal communication modeling and refinement is used to bridge the communication layers and network centric modeling of multiprocessor on chip networks and socket based design will serve the development of platforms for SoC and NoC integration Interconnect centric Design for Advanced SoC and NoC is concluded by two application examples interconnect and memory organization in SoCs for advanced set top boxes and TV and a case study in NoC platform design for more generic applications Electronic Design Automation Laung-Terng Wang, Yao-Wen Chang, Kwang-Ting (Tim) Cheng, 2009-03-11 This book provides broad and comprehensive coverage of the entire EDA flow EDA VLSI practitioners and researchers in need of fluency in an adjacent field will find this an invaluable reference to the basic EDA concepts principles data structures algorithms and architectures for the design verification and test of VLSI circuits Anyone who needs to learn the concepts principles data structures algorithms and architectures of the EDA flow will benefit from this book Covers complete spectrum of the EDA flow from ESL design modeling to logic test synthesis verification physical design and test helps EDA newcomers to get up and running quickly Includes comprehensive coverage of EDA concepts principles data structures algorithms and architectures helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books including Test compression ESL design modeling large scale floorplanning placement routing synthesis of clock and power ground networks helps readers to design develop testable chips or products Includes industry best practices wherever appropriate in most chapters helps readers **On-Chip Communication Architectures** Sudeep Pasricha, Nikil Dutt, 2010-07-28 Over the past avoid costly mistakes decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next

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