

Regular Fabrics In Deep Submicron Integratedcircuit Design

Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer

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Design Fan Mo, Robert King Brayton, 2004 Regular Fabrics in Deep Sub Micron Integrated Circuit Design discusses new approaches to better timing closure and manufacturability of DSM Integrated Circuits The key idea presented is the use of regular circuit and interconnect structures such that area delay can be predicted with high accuracy The co design of structures and algorithms allows great opportunities for achieving better final results thus closing the gap between IC and CAD designers The regularities also provide simpler and possibly better manufacturability. In this book we present not only algorithms for solving particular sub problems but also systematic ways of organizing different algorithms in a flow to solve the design problem as a whole A timing driven chip design flow is developed based on the new structures and their design algorithms which produces faster chips in a shorter time Cross-Talk Noise Immune VLSI Design Using Regular Layout Fabrics Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli, 2012-12-06 This book was motivated by the problems being faced with shrinking IC process feature sizes It is well known that as process feature sizes shrink a host of electrical problems like cross talk electromigration self heat etc are becoming important Cross talk is one of the major problems since it results in unpredictable design behavior In particular it can result in significant delay variation or signal integrity problems in a wire depending on the state of its neighboring wires Typical approaches to tackle the cross talk problem attempt to fix the problem once it is created In our approach we ensure that cross talk is eliminated by design The work described in this book attempts to take an outside the box view and propose a radically different design style This design style first imposes a fixed layout pattern or fabric on the integrated circuit and then embeds the circuit being implemented into this fabric The fabric is chosen carefully in order to eliminate the cross talk problem being faced in modem IC processes With our choice of fabric cross talk between adjacent wires on an IC is reduced by between one and two orders of magnitude In this way the fabric concept eliminates cross talk up front and by design We propose two separate design flows each of which uses the fabric concept to implement logic The first flow uses fabric compliant standard cells as an im plementation vehicle We call these cells fabric cells and they have the same logic functionality as existing standard cells with which they are compared

Interconnect-Centric Design for Advanced SoC and NoC ye have tried to create a comprehensive understanding about on chip interconnect characteristics design methodologies layered views on different abstraction levels and finally about applying the interconnect centric design in system on chip design Traditionally on chip communication design has been done using rather ad hoc and informal approaches that fail to meet some of the challenges posed by next generation SOC designs such as performance and throughput power and energy reliability predictability synchronization and management of concurrency To address these challenges it is critical to take a global view of the communication problem and decompose it along lines that make it more tractable We believe that a layered approach similar to that defined by the communication networks community should also be used for on chip communication design The design issues are handled on physical and

circuit layer logic and architecture layer and from system design methodology and tools point of view Formal communication modeling and refinement is used to bridge the communication layers and network centric modeling of multiprocessor on chip networks and socket based design will serve the development of platforms for SoC and NoC integration Interconnect centric Design for Advanced SoC and NoC is concluded by two application examples interconnect and memory organization in SoCs for advanced set top boxes and TV and a case study in NoC platform design for more generic applications Design Automation Laung-Terng Wang, Yao-Wen Chang, Kwang-Ting (Tim) Cheng, 2009-03-11 This book provides broad and comprehensive coverage of the entire EDA flow EDA VLSI practitioners and researchers in need of fluency in an adjacent field will find this an invaluable reference to the basic EDA concepts principles data structures algorithms and architectures for the design verification and test of VLSI circuits Anyone who needs to learn the concepts principles data structures algorithms and architectures of the EDA flow will benefit from this book Covers complete spectrum of the EDA flow from ESL design modeling to logic test synthesis verification physical design and test helps EDA newcomers to get up and running quickly Includes comprehensive coverage of EDA concepts principles data structures algorithms and architectures helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books including Test compression ESL design modeling large scale floorplanning placement routing synthesis of clock and power ground networks helps readers to design develop testable chips or products Includes industry best practices wherever appropriate in most chapters helps readers avoid costly mistakes On-Chip Communication Architectures Sudeep Pasricha, Nikil Dutt, 2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years Regular Nanofabrics in Emerging Technologies M. Haykel Ben Jamaa, 2011-03-24

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