

Designing Logic Circuits for Probabilistic Computation in the Presence of Noise

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ABSTRACT

As Si CMOS devices are scaled down into the nanoscale regime, current computer architecture approaches are reaching their practical limits. Future nano-architectures will confront devices and interconnections with a large number of inherent defects, which motivates the search for new architectural paradigms. In this paper, we examine probabilistic-based design methodologies for nanoscale computer architectures based on Markov random fields (MRF). The MRF approach can express arbitrary logic circuits and the logic operation is achieved by maximizing the probability of correct state configurations in the logic network depending on the interaction of neighboring circuit nodes. The computation proceeds via probabilistic propagation of states through the circuit. Crucially, the MRF logic can be implemented in modified CMOS-based circuitry that trades off circuit area and operation speed for the crucial fault tolerance and noise immunity. This paper builds on the recent demonstration that significant immunity to faulty individual devices or dynamically occurring signal errors can be achieved by the propagation of state probabilities over an MRF network. In particular, we are interested in CMOS-based circuits that work reliably at very low supply voltages ($V_{DD} = 0.1$ – 0.2 V), where standard CMOS would fail due to thermal and crosstalk noise, and transistor threshold variation. In this paper, we present results for simulated probabilistic test circuits for elementary logic components and well as small circuits taken from the MCNC91 benchmark suite and we show greatly improved noise immunity operating at very low V_{DD} . The MRF framework extends to all levels of a design, where formally optimum probabilistic computation can be implemented as a natural element of the processing structure.

Categories and Subject Descriptors

B.8.1 [Performance and Reliability]: Reliability, Testing, and Fault-tolerance

General Terms

Design, Reliability, Emerging technologies

Keywords

noise immunity, reliability, subthreshold operation, probabilistic computing, Markov random fields, nanodevices

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1. INTRODUCTION

For several decades, mainstream silicon technology has relied on scaling down CMOS transistors following Moore's Law. Thus far, the semiconductor industry has successfully overcome many hurdles, including the current transition to silicon-on-insulator (SOI) technology [1]. Looking to the future, the next major challenges to Si CMOS include new materials (high- κ and low- κ dielectrics [2]), new device geometries (dual-gate or fin-FET devices [3]), and further downscaling of devices and supply voltages with attendant difficulties in manufacturing, power dissipation, and economics of commodity manufacturing [2].

Further into the future, the International Technology Roadmap for Semiconductors (ITRS) predicts that the continued shrinkage of individual transistors will stop, perhaps around 2015, due to unavoidable physical limits, with the ultimate transistor gate length near $L_G \sim 10$ nm [4]. These ultimate transistors will be nanodevices in the true sense of the word. Working $L_G \sim 6$ nm devices have already been reported [5], although there is some debate as to whether the performance gains of such small devices will provide adequate return to justify the enormous fabrication costs. The longer-term prospects of digital computation then diverge into two interrelated areas. On the system side, there are the computer architecture issues arising from the problem of integrating billions of transistors at the lowest possible supply voltage, with tremendous constraints on total power dissipation and device reliability. On the device integration front, there is hope that hybrid systems will emerge, combining CMOS-FET-based digital logic with any number of alternative devices, ranging from analog circuits, to more exotic alternatives (optical sources and detectors, quantum or molecular transistors, carbon nanotube devices, etc.) all on the same chip [6].

Currently, exotic materials — from carbon nanotubes to molecular transistors, to spin-based devices and superconducting junctions, to single-electron devices, all the way to DNA-based computing — are being touted as contenders for computational circuitry. According to some benchmarks, many of these devices are quite successful: they may be faster (tunneling-based devices), carry more current (carbon nanotubes), take up less area (molecular transistors), or have higher logic functionality than CMOS FETs. Yet the key issues of compatibility with the enormous installed base of VLSI fabrication tools and know-how, and with the usual operating parameters (room temperature, low-voltage, ultra-low static power consumption) remain elusive. Instead of targeting the integration of non-CMOS nanodevices into computational logic circuits, we propose to examine the performance of ultimate CMOS transistors in a new computing framework — that of probabilistic computing embedded in a Markov random network. The premises underlying this approach are as follows:

- Any computational scheme involving large numbers of nano-

Reliable Computation In The Presence Of Noise

Tomás Feder



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Reliable Computation in the Presence of Noise S. Winograd, Jack D. Cowan, 1963 **Reliable Computation in the Presence of Noise** International Business Machines Corporation. Research Division, N. Pippenger, 1986 **Reliable Computation by Formulae in the Presence of Noise** International Business Machines Corporation. Research Division, N. Pippenger, 1986 **Coding Approaches to Fault Tolerance in Combinational and Dynamic Systems** Christoforos N. Hadjicostis, 2012-12-06 Coding Approaches to Fault Tolerance in Combinational and Dynamic Systems describes coding approaches for designing fault tolerant systems i.e. systems that exhibit structured redundancy that enables them to distinguish between correct and incorrect results or between valid and invalid states Since redundancy is expensive and counter intuitive to the traditional notion of system design the book focuses on resource efficient methodologies that avoid excessive use of redundancy by exploiting the algorithmic dynamic structure of a particular combinational or dynamic system The first part of Coding Approaches to Fault Tolerance in Combinational and Dynamic Systems focuses on fault tolerant combinational systems providing a review of von Neumann's classical work on Probabilistic Logics including some more recent work on noisy gates and describing the use of arithmetic coding and algorithm based fault tolerant schemes in algebraic settings The second part of the book focuses on fault tolerance in dynamic systems Coding Approaches to Fault Tolerance in Combinational and Dynamic Systems also discusses how in a dynamic system setting one can relax the traditional assumption that the error correcting mechanism is fault free by using distributed error correcting mechanisms The final chapter presents a methodology for fault diagnosis in discrete event systems that are described by Petri net models coding techniques are used to quickly detect and identify failures From the Foreword Hadjicostis has significantly expanded the setting to processes occurring in more general algebraic and dynamic systems The book responds to the growing need to handle faults in complex digital chips and complex networked systems and to consider the effects of faults at the design stage rather than afterwards George Verghese Massachusetts Institute of Technology Coding Approaches to Fault Tolerance in Combinational and Dynamic Systems will be of interest to both researchers and practitioners in the area of fault tolerance systems design and control *3D Nanoelectronic Computer Architecture and Implementation* D. Crawley, K. Nikolic, M. Forshaw, 2020-01-15 It is becoming increasingly clear that the two dimensional layout of devices on computer chips hinders the development of high performance computer systems Three dimensional structures will be needed to provide the performance required to implement computationally intensive tasks 3 D Nanoelectronic Computer Architecture and Implementation reviews the state of the art in nanoelectronic device design and fabrication and discusses the architectural aspects of 3 D designs including the possible use of molecular wiring and carbon nanotube interconnections This is a valuable reference for those involved in the design and development of nanoelectronic devices and technology **The Legacy of John Von Neumann** James G. Glimm, John Impagliazzo, Isadore Singer, 2006-09-08 The ideas of John von

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