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**Todd Lammle, Monica Lammle, James
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web although our aim is to give an understanding of latchup as it occurs in cmos switches similar principles apply to many other cmos devices latchup may be defined as the creation of a low impedance path between power supply rails as a result of triggering a parasitic device

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web in electronics a latch up is a type of short circuit which can occur in an integrated circuit ic more specifically it is the inadvertent creation of a low impedance path between the power supply rails of a mosfet circuit triggering a parasitic structure which disrupts proper functioning of the part possibly even leading to

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web latch up is a condition where a low impedance path is created between a supply pin and ground this condition is caused by a trigger current injection or overvoltage but once activated the low impedance

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web jan 14 2015 what is a latch up early cmos processes suffered a reliability concern that became known as latchup it resulted in circuits either malfunctioning or consuming excessive power and could be either inherent in the design or triggered by voltage spikes on io pads that could forward bias pn junctions they were connected to

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web simply defined latch up is a functional chip failure associated with excessive current going through the chip caused by weak circuit design in some cases latch up can be a temporary condition that can be resolved by power cycle but unfortunately it can also cause a fatal chip failure cmos latch up

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web jan 1 2022 there are two main categories of latch up internal latch up ilu and external latch up elu for the ilu event trigger a few factors include the internal circuit creating supply bounce on chip transmission line reflections or

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web may 10 2020 technically latch up is the phenomena of activating the parasitic bjts in a cmos circuit which forms a low

impedance path between the power and ground terminals this low impedance path draws a large current and heats up the ic integrated chip which cause permanent damage of ic