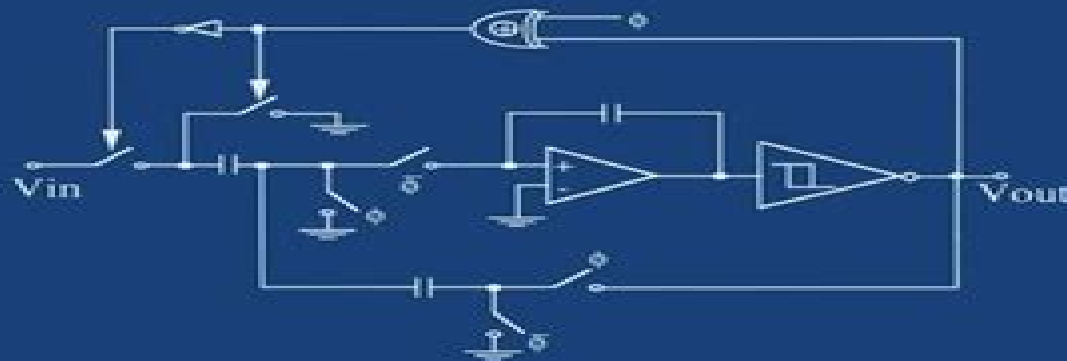


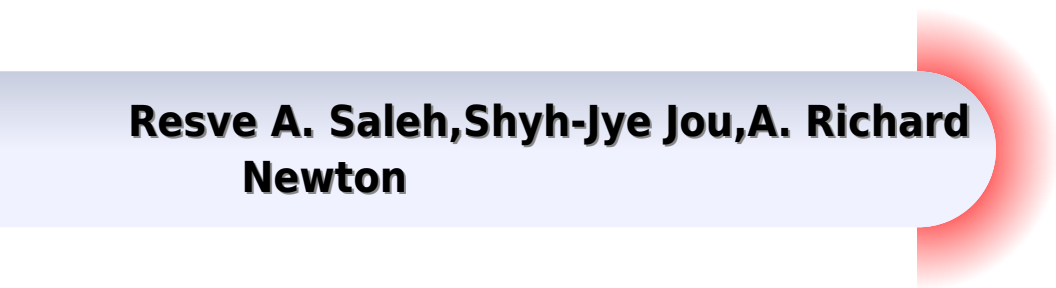
# MIXED-MODE SIMULATION AND ANALOG MULTILEVEL SIMULATION



**Resve Saleh**  
**Shyh-Jye Jou**  
**A. Richard Newton**

# Mixed Mode Simulation And Analog Multilevel Simulation

**Resve A. Saleh, Shyh-Jye Jou, A. Richard  
Newton**



## **Mixed Mode Simulation And Analog Multilevel Simulation:**

Mixed-Mode Simulation and Analog Multilevel Simulation Resve A. Saleh, Shyh-Jye Jou, A. Richard Newton, 1994-08-31 Mixed Mode Simulation and Analog Multilevel Simulation addresses the problems of simulating entire mixed analog digital systems in the time domain A complete hierarchy of modeling and simulation methods for analog and digital circuits is described Mixed Mode Simulation and Analog Multilevel Simulation also provides a chronology of the research in the field of mixed mode simulation and analog multilevel simulation over the last ten to fifteen years In addition it provides enough information to the reader so that a prototype mixed mode simulator could be developed using the algorithms in this book Mixed Mode Simulation and Analog Multilevel Simulation can also be used as documentation for the SPLICE family of mixed mode programs as they are based on the algorithms and techniques described in this book

**Mixed-Mode Simulation and Analog Multilevel Simulation** Resve A. Saleh, Shyh-Jye Jou, A. Richard Newton, 2013-03-09 Mixed Mode Simulation and Analog Multilevel Simulation addresses the problems of simulating entire mixed analog digital systems in the time domain A complete hierarchy of modeling and simulation methods for analog and digital circuits is described Mixed Mode Simulation and Analog Multilevel Simulation also provides a chronology of the research in the field of mixed mode simulation and analog multilevel simulation over the last ten to fifteen years In addition it provides enough information to the reader so that a prototype mixed mode simulator could be developed using the algorithms in this book Mixed Mode Simulation and Analog Multilevel Simulation can also be used as documentation for the SPLICE family of mixed mode programs as they are based on the algorithms and techniques described in this book

**Mixed-Mode Simulation** Resve A. Saleh, A. Richard Newton, 2012-12-06 Our purpose in writing this book was two fold First we wanted to compile a chronology of the research in the field of mixed mode simulation over the last ten to fifteen years A substantial amount of work was done during this period of time but most of it was published in archival form in Masters theses and Ph D dissertations Since the interest in mixed mode simulation is growing and a thorough review of the state of the art in the area was not readily available we thought it appropriate to publish the information in the form of a book Secondly we wanted to provide enough information to the reader so that a proto type mixed mode simulator could be developed using the algorithms in this book The SPLICE family of programs is based on the algorithms and techniques described in this book and so it can also serve as docu mentation for these programs

**ACKNOWLEDGEMENTS** The authors would like to dedicate this book to Prof D O Peder son for inspiring this research work and for providing many years of support and encouragement The authors enjoyed many fruitful discus sions and collaborations with Jim Kleckner Young Kim Alberto Sangiovanni Vincentelli and Jacob White and we thank them for their contributions We also thank the countless others who participated in the research work and read early versions of this book Lillian Beck provided many useful suggestions to improve the manuscript Yun cheng Ju did the artwork for the illustrations

**Simulation and Optimization of Digital Circuits** Vazgen Melikyan, 2018-04-12 This book describes new

fuzzy logic based mathematical apparatus which enable readers to work with continuous variables while implementing whole circuit simulations with speed similar to gate level simulators and accuracy similar to circuit level simulators The author demonstrates newly developed principles of digital integrated circuit simulation and optimization that take into consideration various external and internal destabilizing factors influencing the operation of digital ICs The discussion includes factors including radiation ambient temperature electromagnetic fields and climatic conditions as well as non ideality of interconnects and power rails

**Computer-Aided Design of Analog Integrated Circuits and Systems** Rob A.

Rutenbar, Georges G. E. Gielen, 2002-05-06 The tools and techniques you need to break the analog design bottleneck Ten years ago analog seemed to be a dead end technology Today System on Chip SoC designs are increasingly mixed signal designs With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process Today designers are moving beyond hand crafted one transistor at a time methods They are using new circuit and physical synthesis tools to design practical analog circuits new modeling and analysis tools to allow rapid exploration of system level alternatives and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field this volume collects in one place the essential set of analog CAD papers that form the foundation of today s new analog design automation tools Areas covered are Analog synthesis Symbolic analysis Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck

*Digital Timing Macromodeling for VLSI Design Verification* Jeong-Taek Kong, David V. Overhauser, 2012-12-06

Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques It presents detailed discussion of the various techniques implemented in circuit timing fast timing switch level timing switch level and gate level simulation It also discusses mixed mode simulation and interconnection analysis methods The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the techniques address the device model detail transistor coupling capacitance effective channel length modulation series transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be

accepted in commercial CAD tools by chip designers The techniques presented in Chapters 4-6 can be implemented in other macromodels and are demonstrated using the macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques

**Mechatronic Systems** Georg Pelz, 2003-06-02 Covers the modelling and simulation of mechatronic and micromechatronic systems using HDLs Provides an overview of the design of digital and analog circuitry and software for mechatronic systems Presents practical guidance on both chip and systems design for a wide range of mechatronic applications Focuses on a practical approach to the design and simulation of electronic hardware and components of mechatronic systems

*Test and Design-for-Testability in Mixed-Signal Integrated Circuits* Jose Luis Huertas Díaz, 2010-02-23 Test and Design for Testability in Mixed Signal Integrated Circuits deals with test and design for test of analog and mixed signal integrated circuits Especially in System on Chip SoC where different technologies are intertwined analog digital sensors RF test is becoming a true bottleneck of present and future IC projects Linking design and test in these heterogeneous systems will have a tremendous impact in terms of test time cost and proficiency Although it is recognized as a key issue for developing complex ICs there is still a lack of structured references presenting the major topics in this area The aim of this book is to present basic concepts and new ideas in a manner understandable for both professionals and students Since this is an active research field a comprehensive state of the art overview is very valuable introducing the main problems as well as the ways of solution that seem promising emphasizing their basis strengths and weaknesses In essence several topics are presented in detail First of all techniques for the efficient use of DSP based test and CAD test tools Standardization is another topic considered in the book with focus on the IEEE 1149.4 Also addressed in depth is the connecting design and test by means of using high level behavioural description techniques specific examples are given Another issue is related to test techniques for well defined classes of integrated blocks like data converters and phase locked loops Besides these specification driven testing techniques fault driven approaches are described as they offer potential solutions which are more similar to digital test methods Finally in Design for Testability and Built In Self Test two other concepts that were taken from digital design are introduced in an analog context and illustrated for the case of integrated filters In summary the purpose of this book is to provide a glimpse on recent research results in the area of testing mixed signal integrated circuits specifically in the topics mentioned above Much of the work reported herein has been performed within cooperative European Research Projects in which the authors of the different chapters have actively collaborated It is a representative snapshot of the current state of the art in this emergent field

**The Electronic Design Automation Handbook** Dirk Jansen, 2010-02-23 When I attended college we studied vacuum tubes in our junior year At that time an average radio had vacuum tubes and better ones even seven Then transistors appeared in 1960s A good radio was judged to be one with more transistors Later good radios had 15

20transistors and after that everyone stopped counting transistors Today modern processors runing personal computers have over 10milliontransistorsandmoremillionswillbeaddedevery year The difference between 20 and 20M is in complexity methodology and business models Designs with 20 tr sistors are easily generated by design engineers without any tools whilst designs with 20M transistors can not be done by humans in reasonable time without the help of Prof Dr Gajski demonstrates the Y chart automation This difference in complexity introduced a paradigm shift which required sophisticated methods and tools and introduced design automation into design practice By the decomposition of the design process into many tasks and abstraction levels the methodology of designing chips or systems has also evolved Similarly the business model has changed from vertical integration in which one company did all the tasks from product speci cation to manufacturing to globally distributed client server production in which most of the design and manufacturing tasks are outsourced

**System Design Automation** Renate Merker,Wolfgang Schwarz,2001-03-31 Design automation of electronic and hybrid systems is a steadily growing field of interest and a permanent challenge for researchers in Electronics Computer Engineering and Computer Science System Design Automation presents some recent results in design automation of different types of electronic and mechatronic systems It deals with various topics of design automation ranging from high level digital system synthesis through analogue and heterogeneous system analysis and design up to system modeling and simulation Design automation is treated from the aspects of its theoretical fundamentals its basic approach and its methods and tools Several application cases are presented in detail The book consists of three chapters High Level System Synthesis Digital Hardware Software Systems Here embedded systems distributed systems and processor arrays as well as hardware software codesign are treated Also three special application cases are discussed in detail Analog and Heterogeneous System Design System Approach and Methodology This chapter copes with the analysis and design of hybrid systems comprised of analog and digital electronic and mechanical components System Simulation and Evaluation Methods and Tools In this chapter object oriented Modelling analog system simulation including fault simulation parameter optimization and system validation are regarded The contents of the book are based on material presented at the Workshop System Design Automation SDA 2000 organised by the Sonderforschungsbereich 358 of the Deutsche Forschungsgemeinschaft at TU Dresden

*Formal Semantics for VHDL* Carlos Delgado Kloos,P. Breuer,2012-12-06 It is recognized that formal design and verification methods are an important requirement for the attainment of high quality system designs The field has evolved enormously during the last few years resulting in the fact that formal design and verification methods are nowadays supported by several tools both commercial and academic If different tools and users are to generate and read the same language then it is necessary that the same semantics is assigned by them to all constructs and elements of the language The current IEEE standard VHDL language reference manual LRM tries to define VHDL as well as possible in a descriptive way explaining the semantics in English But rigor and clarity are very hard to maintain in a semantics defined in this way and that

has already given rise to many misconceptions and contradictory interpretations Formal Semantics for VHDL is the first book that puts forward a cohesive set of semantics for the VHDL language The chapters describe several semantics each based on a different underlying formalism two of them use Petri nets as target language and two of them higher order logic Two use functional concepts and finally another uses the concept of evolving algebras Formal Semantics for VHDL is essential reading for researchers in formal methods and can be used as a text for an advanced course on the subject **Digit-Serial**

**Computation** Richard Hartley, Keshab K. Parhi, 2012-12-06 Digital signal processing DSP is used in a wide range of applications such as speech telephone mobile radio video radar and sonar The sample rate requirements of these applications range from 10 KHz to 100 MHz Real time implementation of these systems requires design of hardware which can process signal samples as these are received from the source as opposed to storing them in buffers and processing them in batch mode Efficient implementation of real time hardware for DSP applications requires study of families of architectures and implementation styles out of which an appropriate architecture can be selected for a specified application To this end the digit serial implementation style is proposed as an appropriate design methodology for cases where bit serial systems cannot meet the sample rate requirements and bit parallel systems require excessive hardware The number of bits processed in a clock cycle is referred to as the digit size The hardware complexity and the achievable sample rate increase with increase in the digit size As special cases a digit serial system is reduced to bit serial or bit parallel when the digit size is selected to equal one or the word length respectively A family of implementations can be obtained by changing the digit size parameter thus permitting an optimal trade off between throughput and size Because of their structured architecture digit serial designs lend themselves to automatic compilation from algorithmic descriptions An implementation of this design methodology the Parsifal silicon compiler was developed at the General Electric Corporate Research and Development laboratory Robustness in Automatic Speech Recognition Jean-Claude Junqua, Jean-Paul Haton, 2012-12-06 Foreword

Looking back the past 30 years we have seen steady progress made in the area of speech science and technology I still remember the excitement in the late seventies when Texas Instruments came up with a toy named Speak and Spell which was based on a VLSI chip containing the state of the art linear prediction synthesizer This caused a speech technology fever among the electronics industry Particularly applications of automatic speech recognition were rigorously attempted by many companies some of which were start ups founded just for this purpose Unfortunately it did not take long before they realized that automatic speech recognition technology was not mature enough to satisfy the need of customers The fever gradually faded away In the meantime constant efforts have been made by many researchers and engineers to improve the automatic speech recognition technology Hardware capabilities have advanced impressively since that time In the past few years we have been witnessing and experiencing the advent of the Information Revolution What might be called the second surge of interest to commercialize speech technology as a natural interface for man machine communication began in much better

shape than the first one With computers much more powerful and faster many applications look realistic this time However there are still tremendous practical issues to be overcome in order for speech to be truly the most natural interface between humans and machines

**Modern Methods of Speech Processing** Ravi P. Ramachandran, Richard Mammone, 2012-12-06

The term speech processing refers to the scientific discipline concerned with the analysis and processing of speech signals for getting the best benefit in various practical scenarios These different practical scenarios correspond to a large variety of applications of speech processing research Examples of some applications include enhancement coding synthesis recognition and speaker recognition A very rapid growth particularly during the past ten years has resulted due to the efforts of many leading scientists The ideal aim is to develop algorithms for a certain task that maximize performance are computationally feasible and are robust to a wide class of conditions The purpose of this book is to provide a cohesive collection of articles that describe recent advances in various branches of speech processing The main focus is in describing specific research directions through a detailed analysis and review of both the theoretical and practical settings The intended audience includes graduate students who are embarking on speech research as well as the experienced researcher already working in the field For graduate students taking a course this book serves as a supplement to the course material As the student focuses on a particular topic the corresponding set of articles in this book will serve as an initiation through exposure to research issues and by providing an extensive reference list to commence a literature survey Experienced researchers can utilize this book as a reference guide and can expand their horizons in this rather broad area

**Co-Synthesis of Hardware and Software for Digital Embedded Systems** Rajesh Kumar Gupta, 2012-12-06

Co Synthesis of Hardware and Software for Digital Embedded Systems with a Foreword written by Giovanni De Micheli presents techniques that are useful in building complex embedded systems These techniques provide a competitive advantage over purely hardware or software implementations of time constrained embedded systems Recent advances in chip level synthesis have made it possible to synthesize application specific circuits under strict timing constraints This work advances the state of the art by formulating the problem of system synthesis using both application specific as well as reprogrammable components such as off the shelf processors Timing constraints are used to determine what part of the system functionality must be delegated to dedicated application specific hardware while the rest is delegated to software that runs on the processor This co synthesis of hardware and software from behavioral specifications makes it possible to realize real time embedded systems using off the shelf parts and a relatively small amount of application specific circuitry that can be mapped to semi custom VLSI such as gate arrays The ability to perform detailed analysis of timing performance provides the opportunity of improving the system definition by creating better prototypes Co Synthesis of Hardware and Software for Digital Embedded Systems is of interest to CAD researchers and developers who want to branch off into the expanding field of hardware software co design as well as to digital system designers who are interested in the present power and limitations of CAD techniques and their likely evolution



**Logic Synthesis for Field-Programmable Gate Arrays** Rajeev Murgai, Robert K. Brayton, Alberto L.

Sangiovanni-Vincentelli, 2012-12-06 Short turnaround has become critical in the design of electronic systems. Software programmable components such as microprocessors and digital signal processors have been used extensively in such systems since they allow rapid design revisions. However, the inherent performance limitations of software programmable systems mean that they are inadequate for high performance designs. Designers thus turned to gate arrays as a solution. User programmable gate arrays, field programmable gate arrays (FPGAs) have recently emerged and are changing the way electronic systems are designed and implemented. The growing complexity of the logic circuits that can be packed onto an FPGA chip means that it has become important to have automatic synthesis tools that implement logic functions on these architectures. *Logic Synthesis for Field Programmable Gate Arrays* describes logic synthesis for both look up table (LUT) and multiplexor based architectures with a balanced presentation of existing techniques together with algorithms and the system developed by the authors. Audience: A useful reference for VLSI designers, developers of computer aided design tools and anyone involved in or with FPGAs. High-Performance Digital VLSI Circuit Design Richard X. Gu, Khaled M.

Sharaf, Mohamed I. Elmasry, 2012-12-06 High Performance Digital VLSI Circuit Design is the first book devoted entirely to the design of digital high performance VLSI circuits. CMOS, BiCMOS and bipolar circuits are covered in depth including state of the art circuit structures. Recent advances in both the computer and telecommunications industries demand high performance VLSI digital circuits. Digital processing of signals demands high speed circuit techniques for the GHz range. The design of such circuits represents a great challenge, one that is amplified when the power supply is scaled down to 3.3 V. Moreover, the requirements of low power high performance circuits add an extra dimension to the design of such circuits. *High Performance Digital VLSI Circuit Design* is a self contained text introducing the subject of high performance VLSI circuit design and explaining the speed power tradeoffs. The first few chapters of the book discuss the necessary background material in the area of device design and device modeling respectively. High performance CMOS circuits are then covered, especially the new all N logic dynamic circuits. Propagation delay times of high speed bipolar CML and ECL are developed analytically to give a thorough understanding of various interacting process, device and circuit parameters. High current phenomena of bipolar devices are also addressed as these devices typically operate at maximum currents for limited device area. Different new high performance BiCMOS circuits are presented and compared to their conventional counterparts. These new circuits find direct applications in the areas of high speed adders, frequency dividers, sense amplifiers, level shifters, input output clock buffers and PLLs. The book concludes with a few system application examples of digital high performance VLSI circuits. Audience: A vital reference for practicing IC designers. Can be used as a text for graduate and senior undergraduate students in the area. **Binary Decision Diagrams and Applications for VLSI CAD** Shin-ichi Minato, 2012-12-06

Symbolic Boolean manipulation using binary decision diagrams (BDDs) has been successfully applied to a wide variety of tasks.

particularly in very large scale integration VLSI computer aided design CAD The concept of decision graphs as an abstract representation of Boolean functions dates back to the early work by Lee and Akers In the last ten years BDDs have found widespread use as a concrete data structure for symbolic Boolean manipulation With BDDs functions can be constructed manipulated and compared by simple and efficient graph algorithms Since Boolean functions can represent not just digital circuit functions but also such mathematical domains as sets and relations a wide variety of CAD problems can be solved using BDDs Binary Decision Diagrams and Applications for VLSI CAD provides valuable information for both those who are new to BDDs as well as to long time aficionados from the Foreword by Randal E Bryant Over the past ten years BDDs have attracted the attention of many researchers because of their suitability for representing Boolean functions They are now widely used in many practical VLSI CAD systems this book can serve as an introduction to BDD techniques and it presents several new ideas on BDDs and their applications many computer scientists and engineers will be interested in this book since Boolean function manipulation is a fundamental technique not only in digital system design but also in exploring various problems in computer science from the Preface by Shin ichi Minato

On Optimal Interconnections for VLSI  
 Andrew B. Kahng, Gabriel Robins, 2013-04-17 On Optimal Interconnections for VLSI describes from a geometric perspective algorithms for high performance high density interconnections during the global and detailed routing phases of circuit layout First the book addresses area minimization with a focus on near optimal approximation algorithms for minimum cost Steiner routing In addition to practical implementations of recent methods the implications of recent results on spanning tree degree bounds and the method of Zelikovsky are discussed Second the book addresses delay minimization starting with a discussion of accurate yet algorithmically tractable delay models Recent minimum delay constructions are highlighted including provably good cost radius tradeoffs critical sink routing algorithms Elmore delay optimal routing graph Steiner arborescences non tree routing and wiresizing Third the book addresses skew minimization for clock routing and prescribed delay routing formulations The discussion starts with early matching based constructions and goes on to treat zero skew routing with provably minimum wirelength as well as planar clock routing Finally the book concludes with a discussion of multiple competing objectives i e how to optimize area delay skew and other objectives simultaneously These techniques are useful when the routing instance has heterogeneous resources or is highly congested as in FPGA routing multi chip packaging and very dense layouts Throughout the book the emphasis is on practical algorithms and a complete self contained development On Optimal Interconnections for VLSI will be of use to both circuit designers CAD tool users as well as researchers and developers in the area of performance driven physical design

**Automatic Speech and Speaker Recognition** Chin-Hui Lee, Frank K. Soong, Kuldeep K. Paliwal, 2012-12-06 Research in the field of automatic speech and speaker recognition has made a number of significant advances in the last two decades influenced by advances in signal processing algorithms architectures and hardware These advances include the adoption of a statistical pattern recognition

paradigm the use of the hidden Markov modeling framework to characterize both the spectral and the temporal variations in the speech signal the use of a large set of speech utterance examples from a large population of speakers to train the hidden Markov models of some fundamental speech units the organization of speech and language knowledge sources into a structural finite state network and the use of dynamic programming based heuristic search methods to find the best word sequence in the lexical network corresponding to the spoken utterance Automatic Speech and Speaker Recognition Advanced Topics groups together in a single volume a number of important topics on speech and speaker recognition topics which are of fundamental importance but not yet covered in detail in existing textbooks Although no explicit partition is given the book is divided into five parts Chapters 1 2 are devoted to technology overviews Chapters 3 12 discuss acoustic modeling of fundamental speech units and lexical modeling of words and pronunciations Chapters 13 15 address the issues related to flexibility and robustness Chapter 16 18 concern the theoretical and practical issues of search Chapters 19 20 give two examples of algorithm and implementational aspects for recognition system realization Audience A reference book for speech researchers and graduate students interested in pursuing potential research on the topic May also be used as a text for advanced courses on the subject

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