

MATCHING PROPERTIES OF DEEP SUB-MICRON MOS TRANSISTORS

**Jeroen A. Croon, Willy Sansen
and Herman E. Maes**



Matching Properties Of Deep Sub Micron Mos Transistors

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Matching Properties of Deep Sub-Micron MOS Transistors Jeroen A. Croon, Willy M. C. Sansen, Herman E.

Maes, 2005-03-24 Matching Properties of Deep Sub Micron MOS Transistors examines this interesting phenomenon Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET For analog circuits this determines the trade off between speed power accuracy and yield Furthermore due to the down scaling of device dimensions transistor mismatch has an increasing impact on digital circuits The matching properties of MOSFETs are studied at several levels of abstraction A simple and physics based model is presented that accurately describes the mismatch in the drain current The model is illustrated by dimensioning the unit current cell of a current steering D A converter The most commonly used methods to extract the matching properties of a technology are bench marked with respect to model accuracy measurement accuracy and speed and physical contents of the extracted parameters The physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated This leads to a refinement of the generally applied 1 area law In addition the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance The impact of process parameters on the matching properties is discussed The impact of gate line edge roughness is investigated which is considered to be one of the roadblocks to the further down scaling of the MOS transistor Matching Properties of Deep Sub Micron MOS Transistors is aimed at device physicists characterization engineers technology designers circuit designers or anybody else interested in the stochastic properties of the MOSFET

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Croon, Willy M. C. Sansen, Herman E. Maes, 2008-11-01 Matching Properties of Deep Sub Micron MOS Transistors examines this interesting phenomenon Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET For analog circuits this determines the trade off between speed power accuracy and yield Furthermore due to the down scaling of device dimensions transistor mismatch has an increasing impact on digital circuits The matching properties of MOSFETs are studied at several levels of abstraction A simple and physics based model is presented that accurately describes the mismatch in the drain current The model is illustrated by dimensioning the unit current cell of a current steering D A converter The most commonly used methods to extract the matching properties of a technology are bench marked with respect to model accuracy measurement accuracy and speed and physical contents of the extracted parameters The physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated This leads to a refinement of the generally applied 1 area law In addition the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance The impact of process parameters on the matching properties is discussed The impact of gate line edge roughness is investigated which is considered to be one of the roadblocks to the further down scaling of the MOS transistor Matching Properties of Deep Sub Micron MOS Transistors

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models Discusses the major issue of process variability which severely impacts device and circuit performance in advanced technologies and requires statistical compact models Promotes further research of the evolution and development of compact models for VLSI circuit design and analysis Supplies fundamental and practical knowledge necessary for efficient integrated circuit IC design using nanoscale devices Includes exercise problems at the end of each chapter and extensive references at the end of the book Compact Models for Integrated Circuit Design Conventional Transistors and Beyond is intended for senior undergraduate and graduate courses in electrical and electronics engineering as well as for researchers and practitioners working in the area of electron devices However even those unfamiliar with semiconductor physics gain a solid grasp of compact modeling concepts from this book *Compact Modeling* Gennady Gildenblat,2010-06-22 Most of the recent texts on compact modeling are limited to a particular class of semiconductor devices and do not provide comprehensive coverage of the field Having a single comprehensive reference for the compact models of most commonly used semiconductor devices both active and passive represents a significant advantage for the reader Indeed several kinds of semiconductor devices are routinely encountered in a single IC design or in a single modeling support group Compact Modeling includes mostly the material that after several years of IC design applications has been found both theoretically sound and practically significant Assigning the individual chapters to the groups responsible for the definitive work on the subject assures the highest possible degree of expertise on each of the covered models **Ulsi Front-end Technology: Covering From The First Semiconductor Paper To Cmos Finfet Technology** Wai Shing Lau,2017-08-23 The main focus of this book is ULSI front end technology It covers from the early history of semiconductor science technology from 1874 to state of the art FINFET technology in 2016 Some ULSI back end technology is also covered for example the science and technology of MIM capacitors for analog CMOS has been included in this book *Nanometer Variation-Tolerant SRAM* Mohamed Abu Rahma,Mohab Anis,2012-09-26 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques *Stochastic Process Variation in Deep-Submicron CMOS* Amir

Zjajo,2013-11-19 One of the most notable features of nanometer scale CMOS technology is the increasing magnitude of variability of the key device parameters affecting performance of integrated circuits The growth of variability can be attributed to multiple factors including the difficulty of manufacturing control the emergence of new systematic variation generating mechanisms and most importantly the increase in atomic scale randomness where device operation must be described as a stochastic process In addition to wide sense stationary stochastic device variability and temperature variation existence of non stationary stochastic electrical noise associated with fundamental processes in integrated circuit devices represents an elementary limit on the performance of electronic circuits In an attempt to address these issues Stochastic Process Variation in Deep Submicron CMOS Circuits and Algorithms offers unique combination of mathematical treatment of random process variation electrical noise and temperature and necessary circuit realizations for on chip monitoring and performance calibration The associated problems are addressed at various abstraction levels i e circuit level architecture level and system level It therefore provides a broad view on the various solutions that have to be used and their possible combination in very effective complementary techniques for both analog mixed signal and digital circuits The feasibility of the described algorithms and built in circuitry has been verified by measurements from the silicon prototypes fabricated in standard 90 nm and 65 nm CMOS technology ***IQ Calibration Techniques for CMOS Radio Transceivers*** Sao-Jie

Chen,Yong-Hsiang Hsieh,2006-09-22 The 802.11n wireless standard uses 64 state quadrature amplitude modulation 64 QAM to achieve higher spectral efficiency Consequently the transmitter and receiver require a higher signal to noise ratio with the same level of error rate performance This book offers a fully analog compensation technique without baseband circuitry to control the calibration process Using an 802.11g transceiver design as an example it describes in detail an auto calibration mechanism for I/Q gains and phases imbalance ***High-Speed Photodiodes in Standard CMOS Technology*** Sasa

Radovanovic,Anne-Johan Annema,Bram Nauta,2006-10-11 High speed Photodiodes in Standard CMOS Technology describes high speed photodiodes in standard CMOS technology which allow monolithic integration of optical receivers for short haul communication For short haul communication the cost aspect is important and therefore it is desirable that the optical receiver can be integrated in the same CMOS technology as the rest of the system If this is possible then ultimately a single chip system including optical inputs becomes feasible eliminating EMC and crosstalk problems while data rate can be extremely high The problem of photodiodes in standard CMOS technology is that they have very limited bandwidth allowing data rates up to only 50Mbit per second High speed Photodiodes in Standard CMOS Technology first analyzes the photodiode behaviour and compares existing solutions to enhance the speed After this the book introduces a new and robust electronic equalizer technique that makes data rates of 3Gb/s possible without changing the manufacturing technology The application of this technique can be found in short haul fibre communication optical printed circuit boards but also photodiodes for laser disks ***Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS*** Libin Yao,Michiel Steyaert,Willy M. C.

Sansen,2006-02-06 this book is not suitable for the bookstore catalogue Design of Very High-Frequency Multirate Switched-Capacitor Circuits Seng-Pan U,Rui Paulo Martins,José Epifânio da Franca,2006 Design of Very High Frequency Multirate Switched Capacitor Circuits presents the theory and the corresponding CMOS implementation of the novel multirate sampled data analog interpolation technique which has its great potential on very high frequency analog front end filtering due to its inherent dual advantage of reducing the speed of data converters and DSP core together with the specification relaxation of the post continuous time filtering This technique completely eliminates the traditional phenomenon of sampled and hold frequency shaping at the lower input sampling rate Also in order to tackle physical IC imperfections at very high frequency the state of the art circuit design and layout techniques for high speed Switched Capacitor SC circuits are comprehensively discussed Optimum circuit architecture tradeoff analysis Simple speed and power trade off analysis of active elements High order filtering response accuracy with respect to capacitor ratio mismatches Time interleaved effect with respect to gain and offset mismatch Time interleaved effect with respect to timing skew and random jitter with non uniformly holding Stage noise analysis and allocation scheme Substrate and supply noise reduction Gain and offset compensation techniques High bandwidth low power amplifier design and layout Very low timing skew multiphase generation Two tailor made optimum design examples in CMOS are presented The first one achieves a 3 stage 8 fold SC interpolating filter with 5 5MHz bandwidth and 108MHz output sampling rate for a NTSC PAL CCIR 601 digital video at 3 V Another is a 15 tap 57MHz SC FIR bandpass interpolating filter with 4 fold sampling rate increase to 320MHz and the first time embedded frequency band up translation for DDFS system at 2 5V The corresponding chip prototype achieves so far the highest operating frequency highest filter order and highest center frequency with highest dynamic range under the lowest supply voltage when compared to the previously reported high frequency SC filters in CMOS **Dynamic**

Characterisation of Analogue-to-Digital Converters Dominique Dallet,José Machado da Silva,2006-03-08 The Analogue to digital converter ADC is the most pervasive block in electronic systems With the advent of powerful digital signal processing and digital communication techniques ADCs are fast becoming critical components for system s performance and flexibility Knowing accurately all the parameters that characterise their dynamic behaviour is crucial on one hand to select the most adequate ADC architecture and characteristics for each end application and on the other hand to understand how they affect performance bottlenecks in the signal processing chain Dynamic Characterisation of Analogue to Digital Converters presents a state of the art overview of the methods and procedures employed for characterising ADCs dynamic performance behaviour using sinusoidal stimuli The three classical methods histogram sine wave fitting and spectral analysis are thoroughly described and new approaches are proposed to circumvent some of their limitations This is a must have compendium which can be used by both academics and test professionals to understand the fundamental mathematics underlining the algorithms of ADC testing and as an handbook to help the engineer in the most important and critical details

for their implementation **RF Power Amplifiers for Mobile Communications** Patrick Reynaert, Michiel Steyaert, 2006-11-18 This book tackles both high efficiency and high linearity power amplifier PA design in low voltage CMOS. With its emphasis on theory, design and implementation, the book offers a guide for those actively involved in the design of fully integrated CMOS wireless transceivers. Offering mathematical background as well as intuitive insight, the book is essential reading for RF design engineers and researchers and is also suitable as a text book **Adaptive Low-Power Circuits for Wireless Communications** Aleksandar Tasic, Wouter A. Serdijn, John R. Long, 2007-03-06 Adaptive radio transceivers require a comprehensive theoretical framework in order to optimize their performance. Adaptive Low Power Circuits for Wireless Communications provides this framework with a discussion of joint optimization of Noise Figure and Input Intercept Point in receiver systems. Original techniques to optimize voltage controlled oscillators and low noise amplifiers to minimize their power consumption while maintaining adequate system performance are also provided. The experimental results presented at the end of the book confirm the utility of the proposed techniques **Wide-Bandwidth High Dynamic Range D/A Converters** Konstantinos Doris, Arthur H.M. van Roermund, Domine Leenaerts, 2006-01-12 IGH SPEED Digital to Analog D/A converters are essential components in digital communication systems providing the necessary conversion of signals encoding information in bits to signals encoding information in their amplitude vs time domain characteristics. In general, they are parts of a larger system, the interface, which consists of several signal conditioning circuits. Dependent on where the converter is located within the chain of circuits in the interface, signal processing operations are partitioned in those realized with digital techniques and those with analog. The rapid evolution of CMOS technology has established implicit and explicit trends related to the interface and in particular to the D/A converter. The implicit relationship comes via the growth of digital systems. First, it is a global trend with respect to all interface circuits that increasing operating frequencies of digital systems place a similar demand for the interface circuits. The second trend takes place locally within the interface. Initially, the D/A converter was placed at the beginning of the interface chain and all signal conditioning was implemented in the analog domain after the D/A conversion. The increasing flexibility and robustness of digital signal processing shifted the D/A converter closer to the end point of the chain where the demands for high quality high frequency operation are very high **Sigma Delta A/D Conversion for Signal Conditioning** Kathleen Philips, Arthur H.M. van Roermund, 2006-05-05 1.1 Background Moore's Law predicts a decrease by a factor of two in the feature size of CMOS technology every three years and has been valid for years. It implies a doubling of the operation speed and a four times higher transistor count per unit of area every three years. The combination leads to an eight times higher processing capability per unit of area. This ongoing miniaturization allows the integration of complex electronic systems with millions of transistors. Very Large Scale Integration enables the integration of electronic systems. An electronic system. A generic picture of an integrated electronic system is shown in fig. 1.1. The heart of the system is the signal processing core. This core

supports a wide variety of functions such as customization and programmability of multiple applications channel coding the definition of the user interface etc These functions are enabled by DSP a controller CPU and various blocks of memory In advanced ICs these blocks provide almost all signal processing and usually dominate in the overall power and area consumption of integrated systems The huge data rates involved require high speed busses for communication between these blocks A power management unit fuels the system by providing the appropriate supply voltages and currents

Calibration Techniques in Nyquist A/D Converters Hendrik van der Ploeg, Bram Nauta, 2006-09-13 This book analyses different A/D converter architectures with an emphasis on the maximum achievable power efficiency It also provides an accessible overview of the state of the art in calibration techniques for Nyquist A/D converters The calibration techniques presented are applicable to other analog to digital systems such as those applied in integrated receivers They allow implementation without introducing a speed or power penalty

CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom Rocío Río Fernández, Fernando Medeiro Hidalgo, Belén Pérez Verdú, José Manuel Rosa Utrera, Ángel Rodríguez-Vázquez, 2006-09-03 Institutional book not really for bookstore catalogue The book contains valuable information structured to provide insight on how to design SC sigma delta modulators It presents architectures circuits models methods and practical considerations for the design of high performance low pass switched capacitor SC sigma delta A/D interfaces for mixed signal CMOS ASICs The main focus of the book is on cascade architectures It differs from other books in the complete in depth coverage of SC circuit errors

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