

Reconfigurable Processor Array A Bit Sliced Parallel Computer (USA)

Rushton, A.

Reconfigurable Processor Array A Bit Sliced Parallel Computer Usa

Walter B. Meigs,E. Larsen,R. Meigs



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Reconfigurable Processor Array A Bit Sliced Parallel Computer (Usa) A. Rushton,1991-02 **Principles of Auditing/Study Guide** Walter B. Meigs,E. Larsen,R. Meigs,1988-12-01 **Reconfigurable Processor-array** Andrew Rushton,1989 This book investigates enhancements to the conventional bit serial PE with the aim of improving its performance in situations where the small grain parallelism of a single instruction stream multiple data stream SIMD class parallel computer architecture is inefficient **Languages and Compilers for Parallel Computing** Lawrence Rauchwerger,2019-11-19 This book constitutes the proceedings of the 30th International Workshop on Languages and Compilers for Parallel Computing LCPC 2017 held in College Station TX USA in October 2017 The 17 full papers presented together with abstracts of 5 keynote talks 11 invited speakers and 4 poster papers in this volume were carefully reviewed and selected from 26 submissions LCPC encourages submissions that go outside its original scope of scientific computing to diverse areas that are enable or enhanced by the power of parallel systems such as mobile computing big data relevant aspects of machine learning data centers cognitive computing etc LCPC strongly encourages personal interaction and technical discussions along the initial material **The Publishers' Trade List Annual** ,1995 **Forthcoming Books** Rose Army,1989-05 **Bibliographic Guide to Computer Science** ,1990 *Parallelogram International* ,1990
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